NTSC/PAL Encoders

The HMP8154 and HMP8156A NTSC and PAL encoders are designed for use in systems requiring the generation of high-quality NTSC and PAL video from digital image data.

YCbCr or RGB digital video data drive the P0-P23 inputs. Overlay inputs are processed and the data is 2x upsampled. The Y data is optionally lowpass filtered to 6MHz and drives the Y analog output. Cb and Cr are each lowpass filtered to 1.3MHz, quadrature modulated, and summed. The result drives the C analog output. The digital Y and C data are also added together and drive the two composite analog outputs.

The YCbCr data may also be converted to RGB data to drive the DACs, allowing support for analog component RGB and the European SCART connector.

The DACs can drive doubly-terminated (37.5Ω) lines, and run at a 2x oversampling rate to simplify the analog output filter requirements. Any unused DACs may be powered down to reduce power consumption.

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HMP8154CN	HMP8154 CN	0 to 70	64 Ld PQFP	Q64.14x14
HMP8156ACN	HMP8156 ACN	0 to 70	64 Ld PQFP	Q64.14x14
HMP8156ACNZ (See Note)	HMP8156 ACNZ	0 to 70	64 Ld PQFP (Pb-free)	Q64.14x14
HMP8154EVAL1 HMP8156EVAL1	Daughter/Stand-Alone Card Evaluation Platform*			
HMP8156EVAL2	Frame Grabber Evaluation Platform*			

*Described in the Applications Section

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
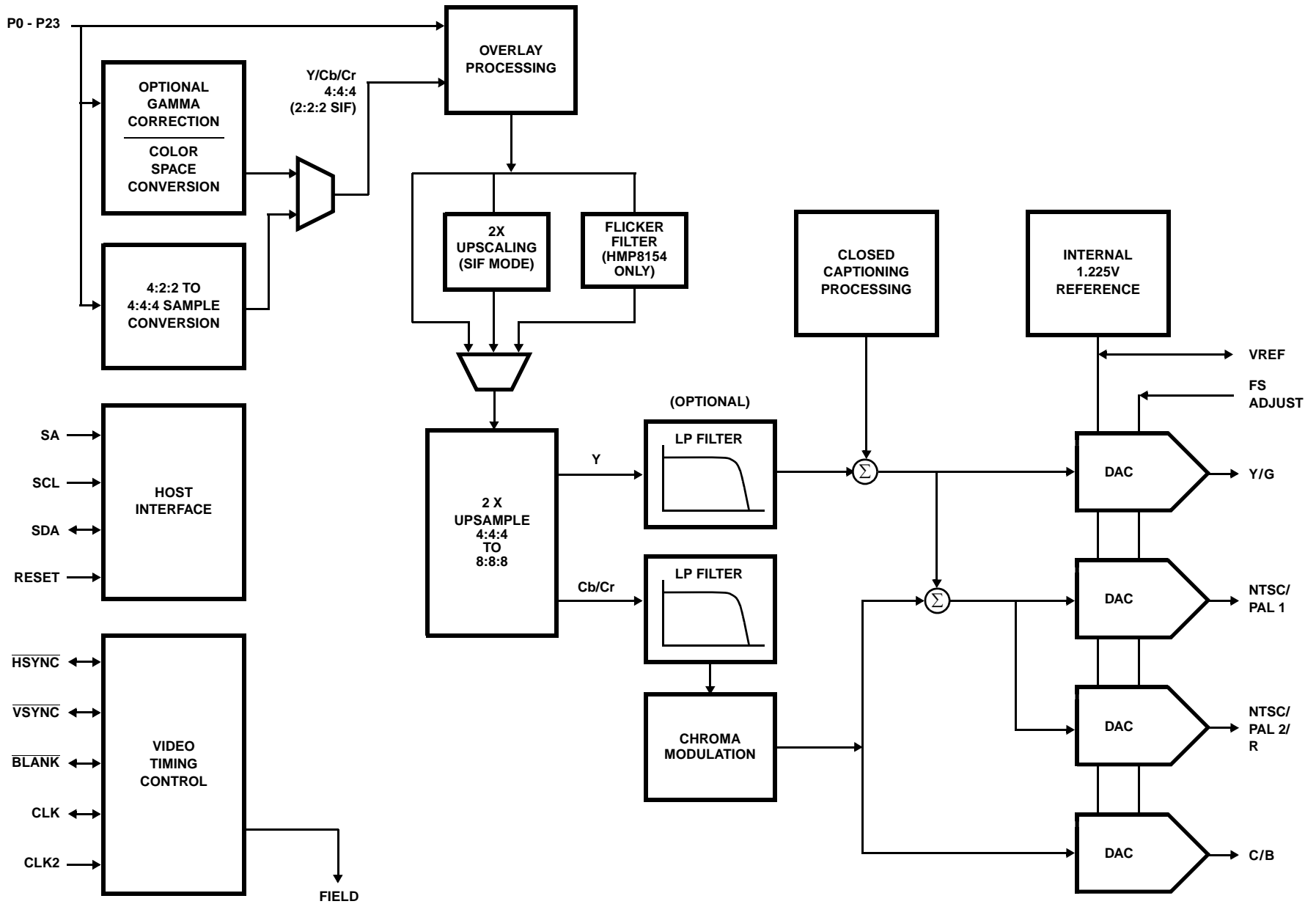
Features

- (M) NTSC and (B, D, G, H, I, M, N, CN) PAL Operation
- ITU-R BT.601 and Square Pixel Operation
- Digital Input Formats
  - 4:2:2 YCbCr
    - 8-Bit or 16-Bit
  - 4:4:4 RGB
    - 16-Bit (5, 6, 5) or 24-Bit (8, 8, 8)
    - Linear or Gamma-Corrected
  - 8-Bit BT.656
- Overlay Mixing
  - 7 Colors
  - Internal, External, or Hard Mixing Control
- Analog Output Formats
  - Y/C + Two Composite
  - RGB + Composite (SCART)
- Flexible Video Timing Control
  - Timing Master or Slave
  - Programmable Input Sync Timing
  - Selectable Polarity on Each Control Signal
  - Programmable Blank Output Timing
  - Field Output
- Closed Caption Encoding for NTSC and PAL
- 2x Upscaling of SIF Video
- Three Line Vertical Flicker Filter (HMP8154 only)
- Four 2x Oversampling, 10-Bit DACs with Power Down
- I^{2}C Interface
- Verilog Models Available
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Multimedia PCs
- Video Conferencing
- Video Editing
- Related Products
  - NTSC/PAL Encoders: HMP8170-HMP8173
  - HMP8190/91
  - NTSC/PAL Decoders: HMP8112A, HMP8115, HMP8116, HMP8130/31

Functional Block Diagram

P0 - P23

OPTIONAL GAMMA CORRECTION

COLOR SPACE CONVERSION

Y/Cb/Cr 4:4:4 (2:2:2 SIF)

OVERLAY PROCESSING

4:2:2 TO 4:4:4 SAMPLE CONVERSION

2X UPSCALING (SIF MODE)

FLICKER FILTER (HMP8154 ONLY)

CLOSED CAPTIONING PROCESSING

INTERNAL 1.225V REFERENCE

VREF

FS ADJUST

SA

SCL

SDA

RESET

HOST INTERFACE

2 X UPSAMPLE 4:4:4 TO 8:8:8

Y

(OPTIONAL)

LP FILTER

Σ

DAC

Y/G

HSYNC

VSYNC

BLANK

CLK

CLK2

VIDEO TIMING CONTROL

FIELD

Cb/Cr

LP FILTER

Σ

DAC

NTSC/ PAL 1

CHROMA MODULATION

DAC

NTSC/ PAL 2/ R

DAC

C/B

Functional Operation

The HMP8154 and HMP8156A are fully integrated digital encoders. Either accepts digital video input data and generates four analog video output signals. The input data format is selectable and includes YCbCr, RGB, and overlay data. The outputs are configurable to be either two composite video signals and Y/C (S-Video) or one composite and component RGB video.

The HMP8154/HMP8156A accepts pixel data in one of several formats and transforms it into 4:4:4 sampled luminance and chrominance (YCbCr) data. If enabled, the encoder also mixes overlay data with the input data. The encoder then interpolates the YCbCr data to twice the pixel rate and low pass filters it to match the bandwidth of the video output format. If enabled, the encoder also adds Closed Captioning information to the Y data. At the same time, the encoder modulates the chrominance data with a digitally synthesized subcarrier. Finally, the encoder outputs luminance, chrominance, and their sum as analog signals using 10-bit D/A converters.

The HMP8154/HMP8156A provides operating modes to support all versions of the NTSC and PAL standards and accepts full and SIF size input data with rectangular (ITU-R BT.601) and square pixel aspect ratios. It operates from a single clock at twice the pixel clock rate determined by the operating mode.

The HMP8154/HMP8156A's video timing control is flexible. It may operate as the master generating the system's video timing control signals or it may accept external timing controls. The polarity of the timing controls and the number of active pixels and lines are programmable.

The HMP8154 provides optional vertical flicker reduction. When enabled, the encoder passes the pixel data after overlay processing through a three line flicker filter.

Pixel Data Input Formats

The HMP8154 accepts pixel data via the P0-P23 input pins. The definition of each pixel input pin is determined by the input format selected in the input format register. The definition for each mode is shown in Table 1.

YCbCr Pixel Data

The HMP8154/HMP8156A accepts 4:2:2 sampled YCbCr input data. The luminance and color difference signals are each 8 bits, scaled 0 to 255. The nominal range for Y is 16 (black) to 235 (white). Y values less than 16 are clamped to 16; values greater than 235 are processed normally. The nominal range for Cb and Cr is 16 to 240 with 128 representing zero. Cb and Cr values outside their nominal range are processed normally. Note that when converted to the analog outputs, some combinations of YCbCr outside their nominal ranges would generate a composite video signal

larger than the analog output limit. The composite signal will be clipped but the S-video outputs (Y and C) will not be.

The color difference signals are time multiplexed into one 8-bit bus beginning with a Cb sample. The Y and CbCr busses may be input in parallel (16-bit mode) or may be time multiplexed and input as a single bus (8-bit mode). The single bus may also contain SAV and EAV video timing reference codes (BT.656 mode).

RGB Data

The HMP8154/HMP8156A accepts 4:4:4 sampled RGB component video input data. The color signals may be (8,8,8) for 24-bit mode or (5,6,5) for 16-bit mode. In 24-bit mode, they are scaled 0 to 255, black to white. In 16-bit mode, the encoder left shifts the input so that it has the same scale as 24-bit input. The RGB data may be linear or gamma corrected; if enabled, the encoder will gamma correct the input data.

Overlay Data

The HMP8154/HMP8156A accepts 5 bits of pixel overlay input data and combines it with the input pixel data. The data specifies an overlay color and the fractions of the new and original colors to be summed.

Blue Screen Generation

In blue screen mode, the HMP8154/HMP8156A ignores the pixel input data and generates a solid, blue screen. The overlay inputs may be used to place information over the blue screen.

Input Processing

Color Space Conversion

For linear RGB input formats, the encoder applies gamma-correction using a selectable gamma value of 1/2.2 or 1/2.8. The gamma-corrected RGB data from either the correction function in linear mode or the input port otherwise is converted to 4:4:4 sampled YCbCr data.

For the YCbCr input formats, the encoder converts the 4:2:2 sampled data to 4:4:4 sampled data. The conversion is done by 2x upsampling the Cb and Cr data. The upsampling function uses linear interpolation.

Overlay Processing

The HMP8154/HMP8156A accepts overlay data via the OL0-OL2, M0, and M1 pins. Overlay mixing is done using the 4:4:4 YCbCr pixel data from the color space converter. The YCbCr data following overlay processing is used as input data by the video processing functions.

The OL0-OL2 inputs select the color to be mixed with the pixel data. Overlay colors 1-7 are standard color bar colors. Overlay color 0 is special and disables mixing on a pixel-by-pixel basis. The overlay color palette is shown in Table 2.

TABLE 1. PIXEL DATA INPUT FORMATS

PIN NAME	16-BIT 4:2:2 YCBCR	8-BIT 4:2:2 YCBCR	BT.656	BLUE SCREEN	16-BIT RGB (5, 6, 5)	24-BIT RGB
P0	Cb0, Cr0	Ignored			B0	B0
P1	Cb1, Cr1				B1	B1
P2	Cb2, Cr2				B2	B2
P3	Cb3, Cr3				B3	B3
P4	Cb4, Cr4				B4	B4
P5	Cb5, Cr5				G0	B5
P6	Cb6, Cr6				G1	B6
P7	Cb7, Cr7				G2	B7
P8	Y0	Y0, Cb0, Cr0	YCbCr Data, SAV and EAV Sequences	Ignored	G3	G0
P9	Y1	Y1, Cb1, Cr1			G4	G1
P10	Y2	Y2, Cb2, Cr2			G5	G2
P11	Y3	Y3, Cb3, Cr3			R0	G3
P12	Y4	Y4, Cb4, Cr4			R1	G4
P13	Y5	Y5, Cb5, Cr5			R2	G5
P14	Y6	Y6, Cb6, Cr6			R3	G6
P15	Y7	Y7, Cb7, Cr7			R4	G7
P16		OL0				R0
P17		OL1				R1
P18		OL2				R2
P19		M0				R3
P20		M1				R4
P21		-				R5
P22		-				R6
P23		-				R7

TABLE 2. OVERLAY COLOR PALETTE

OL2-OL0	COLOR
000	Pixel Data
001	75% Blue
010	75% Red
011	75% Magenta
100	75% Green
101	75% Cyan
110	75% Yellow
111	100% White

Note that overlay capability is not available when the 24-bit RGB input format is used.

The encoder provides 4 methods for mixing the overlay data with the pixel data: disabled, external mixing, internal mixing and no mixing. The method used is selected in the input format control register.

Overlay Mixing: Disabled

When overlay mixing is disabled, the OL0-OL2, M0, and M1 inputs are ignored and the pixel data is not changed.

Overlay Mixing: External

When external overlay mixing is selected, mixing of overlay data and pixel data is controlled by the M1 and M0 inputs. M1 and M0 indicate the mixing level between the pixel inputs and the overlay inputs, on a pixel-by-pixel basis. M1 and M0 are ignored if OL2-OL0 = 000. Otherwise, they select the percentage of each color to sum as shown in Table 3.

TABLE 3. OVERLAY MIXING FACTORS

M1, M0	% OVERLAY COLOR	% PIXEL COLOR
00	0	100
01	12.5	87.5
10	87.5	12.5
11	100	0

In external mixing mode, there is no minimum number of pixels an overlay color or pixel color must be selected. The mixing level may also vary at any rate.

Overlay Mixing: Internal

Mixing of overlay and pixel data may also be controlled internally, and the M1 and M0 input pins are ignored. A transition from pixel data to overlays, from overlays to pixel data, or between different overlay colors triggers the mixing function. An overlay color must be selected for a minimum of three pixels for proper overlay operation in this mode. Internal overlay mixing should not be used with the BT.656 input format.

When going from pixel to overlay data, mixing starts one pixel before the selection of the overlay color (OL2-OL1 != 000). The first pixel output before the overlay uses 12.5% overlay color plus 87.5% pixel color. The next output is aligned with the selection of the overlay color and uses 87.5% overlay color plus 12.5% pixel color. Additional outputs use 100% overlay color.

When going from overlay to pixel data, mixing starts one pixel before the selection of the pixel color (OL2-OL0 = 000).

The last pixel output of the overlay uses 87.5% overlay color plus 12.5% pixel color. The next output uses 12.5% overlay color plus 87.5% pixel color. Additional outputs use 100% pixel color.

When going from one overlay color to another, mixing starts one pixel before the selection of the new overlay color, and uses 12.5% new overlay color plus 87.5% old overlay color. The next output is aligned with the selection of the new overlay color and uses 87.5% new overlay color plus 12.5% old overlay color. Additional outputs use 100% new overlay color.

Overlay Mixing: No Mixing

With no overlay mixing selected, whenever the OL0-OL2 inputs are non-zero, the overlay color is displayed. The M0 and M1 inputs are ignored, and no internal mixing is done. Essentially, this is a hard switch between overlay and pixel data. In this mode, there is no minimum number of pixels an overlay color or pixel color must be selected.

2X Upscaling Processing

Following overlay processing, 2X upscaling may optionally be applied to the pixel data. In this mode, the HMP8154/HMP8156A accepts NTSC (PAL) SIF resolution video at 59.94 (50) *frames* per second and generates standard interlaced video with 262.5 (312.5) lines per field at 59.94 (50) *fields* per second. This mode of operation allows SIF video to be upscaled to full resolution and recorded on a VCR or displayed on a TV. SIP upscaling may be used to simplify PC to TV applications.

The input pixel data rate is reduced by half when 2X upscaling is enabled. The color space conversion generates, and the overlay mixer uses, 2:2:2 YCbCr data instead of 4:4:4 data. For rectangular pixel NTSC and PAL video, the input rate is 6.75MHz during the active portion of each line instead of 13.5MHz. Example SIF input resolutions and resulting output resolutions are shown in Table 4.

TABLE 4. TYPICAL RESOLUTIONS FOR 2X UPSCALING

INPUT ACTIVE RESOLUTION	OUTPUT ACTIVE RESOLUTION
352 x 240	704 x 480
352 x 288	704 x 576
320 x 240	640 x 480
384 x 288	768 x 576

The HMP8154/HMP8156A performs horizontal 2X upscaling by linear interpolation. The vertical scaling is done by line duplication. For typical line duplication, the same frame of SIF pixel input data is used for both the odd and even fields. Note that a frame of SIF size input has about the same number of lines as a field of full size input.

After 2X upscaling, the input is 4:4:4 YCbCr data ready for video processing. Flicker filtering is not available when 2X upscaling is enabled.

Flicker Filter Processing

Following overlay processing, vertical flicker filtering may optionally be applied to the pixel data by the HMP8154. The HMP8156A does not provide flicker filter capability. In flicker filter mode, the HMP8154 accepts non-interlaced NTSC (PAL) full resolution video with 525 (625) lines per frame at 59.94 (50) *frames* per second. It generates standard interlaced video with 262.5 (312.5) lines per field at 59.94 (50) *fields* per second.

Each frame of non-interlaced video is vertically low pass filtered and used to generate either an odd or even field of video. This mode of operation reduces flickering caused by image details that are less than two pixels high.

Since an entire frame of input is used to generate one field of output, the input pixel data rate is doubled when the flicker filter is enabled. The encoder must receive two lines of data during each line time. For rectangular pixel NTSC and PAL video, the input rate is 27.0MHz during the active portion of each line instead of 13.5MHz. Because of the high input data rate, 8-bit YCbCr and BT.656 input formats and 2X upscaling of SIF input may not be used when the flicker filter is enabled.

The HMP8154 uses internal line stores and a 3 tap FIR filter to reduce flickering. The filter coefficients are 0.25, 0.5, and 0.25. At the start and end of each field, the coefficients are modified to compensate for the insufficient number of lines available for processing.

When filtering is enabled, there is an additional two line time delay through the encoder. After flicker filtering, the input is 4:4:4 YCbCr data ready for video processing. 2X upscaling is not available when the flicker filter is enabled.

Pixel Input and Control Signal Timing

The pixel input timing and the video control signal input/output timing of the HMP8154/HMP8156A depend on the part's operating mode. The periods when the encoder samples its inputs and generates its outputs are summarized in Table 5.

Figures 1-12 show the timing of CLK, CLK2, $\overline{BLANK}$, and the pixel and overlay input data with respect to each other. $\overline{BLANK}$ may be an input or an output; the figures show both. When it is an input, $\overline{BLANK}$ must arrive coincident with the pixel and overlay input data; all are sampled at the same time.

When $\overline{BLANK}$ is an output, its timing with respect to the pixel and overlay inputs depends on the blank timing select bit in the timing_I/O_1 register. If the bit is cleared, the HMP8154/HMP8156A deasserts $\overline{BLANK}$ one CLK cycle before it samples the pixel and overlay inputs. As shown in the timing figures, the encoder samples the inputs 1-7 CLK2 periods after negating $\overline{BLANK}$, depending on the operating mode.

If the bit is set, the encoder deasserts $\overline{BLANK}$ during the same CLK cycle in which it samples the input data. In effect, the input data must arrive one CLK cycle earlier than when the bit is cleared. This mode is not shown in the figures.

HMP8154, HMP8156A

TABLE 5. PIXEL INPUT AND CONTROL SIGNAL I/O TIMING

INPUT FORMAT	MODE (NOTE 1)	INPUT PORT SAMPLING		VIDEO TIMING CONTROL (NOTE 2)		CLK FREQUENCY	
		PIXEL DATA	OVERLAY DATA	INPUT SAMPLE	OUTPUT ON	INPUT	OUTPUT
8-Bit YCbCr	Norm	Every rising edge of CLK2	Same edge that latches Y	Every rising edge of CLK2	Any rising edge of CLK2	Ignored	One-half CLK2
	2X	Rising edge of CLK2 when CLK is low.	Same edge that latches Y data	Rising edge of CLK2 when CLK is low.	Rising edge of CLK2 when CLK is high.	One-half CLK2	
	FF	Not Available					
16-Bit YCbCr, 16-Bit RGB, or 24-Bit RGB	Norm	Rising edge of CLK2 when CLK is low			Rising edge of CLK2 when CLK is high.	One-half CLK2	
	2X	2nd rising edge of CLK2 when CLK is low			Either rising CLK2 edge when CLK is high	One-fourth CLK2	
	FF	Every rising edge of CLK2	Same edge that latches Y	Every rising edge of CLK2	Any rising edge of CLK2	Ignored	One-half CLK2
BT.656	Norm	Every rising edge of CLK2	Same edge that latches Y	Not Allowed	Any rising edge of CLK2	Ignored	One-half CLK2
	2X	Not Available					
	FF	Not Available					

NOTES:

1. Encoder operating modes:
   Norm = Full size input, Flicker filter disabled.
   2X = SIF size input, Flicker filter disabled.
   FF = Full size input, Flicker filter enabled.
   (2X upscaling and flicker filtering are mutually exclusive.)

2. Video timing control signals include $\overline{HSYNC}$, $\overline{VSYNC}$, $\overline{BLANK}$ and FIELD. The sync and blanking I/O directions are independent; FIELD is always an output.

Normal 8-Bit YCbCr Format

When 8-bit YCbCr format is selected and 2X upscaling or flicker filtering is not enabled, the data is latched on each rising edge of CLK2. The pixel data must be [Cb Y Cr Y' Cb Y Cr Y' . . .], with the first active data each scan line being Cb data. Overlay data is latched when the Y input data is latched. The pixel and overlay input timing is shown in Figure 1.

As inputs, $\overline{BLANK}$, $\overline{HSYNC}$, and $\overline{VSYNC}$ are latched on each rising edge of CLK2. As outputs, $\overline{BLANK}$, $\overline{HSYNC}$, and $\overline{VSYNC}$ are output following the rising edge of CLK2. If the CLK pin is configured as an input, it is ignored. If configured as an output, it is one-half the CLK2 frequency.

8-Bit YCbCr Format with 2X Upscaling

When 8-bit YCbCr format is selected and 2X upscaling is enabled, the data is latched on the rising edge of CLK2 while CLK is low. The pixel data must be [Cb Y Cr Y' Cb Y Cr Y'. . .], with the first active data each scan line being Cb data. Overlay data is latched on the rising edge of CLK2 that latches Y pixel input data. The pixel and overlay input timing is shown in Figure 2.

As inputs, $\overline{BLANK}$, $\overline{HSYNC}$, and $\overline{VSYNC}$ are latched on the rising edge of CLK2 while CLK is low. As outputs, $\overline{HSYNC}$, $\overline{VSYNC}$, and $\overline{BLANK}$ are output following the rising edge of CLK2 while CLK is high. In this mode of operation, CLK is one-half the CLK2 frequency.
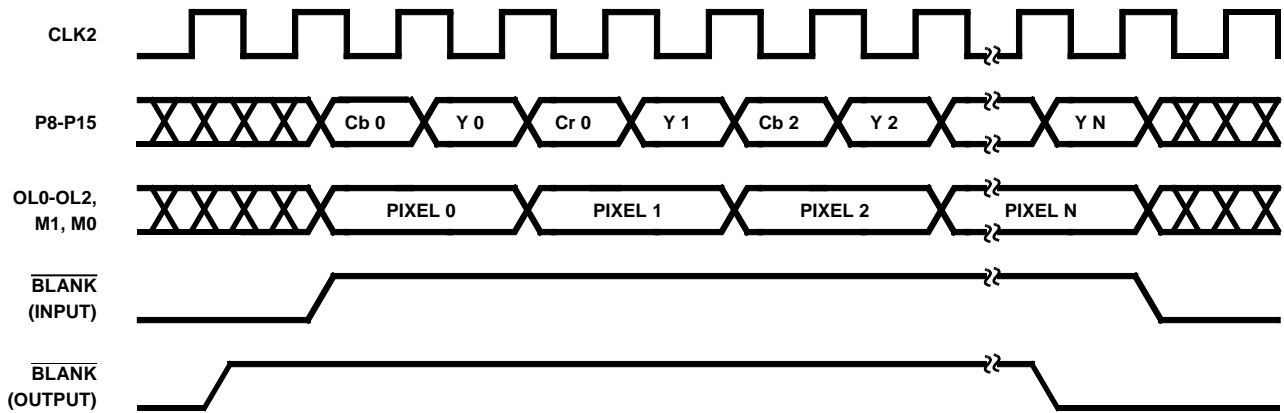
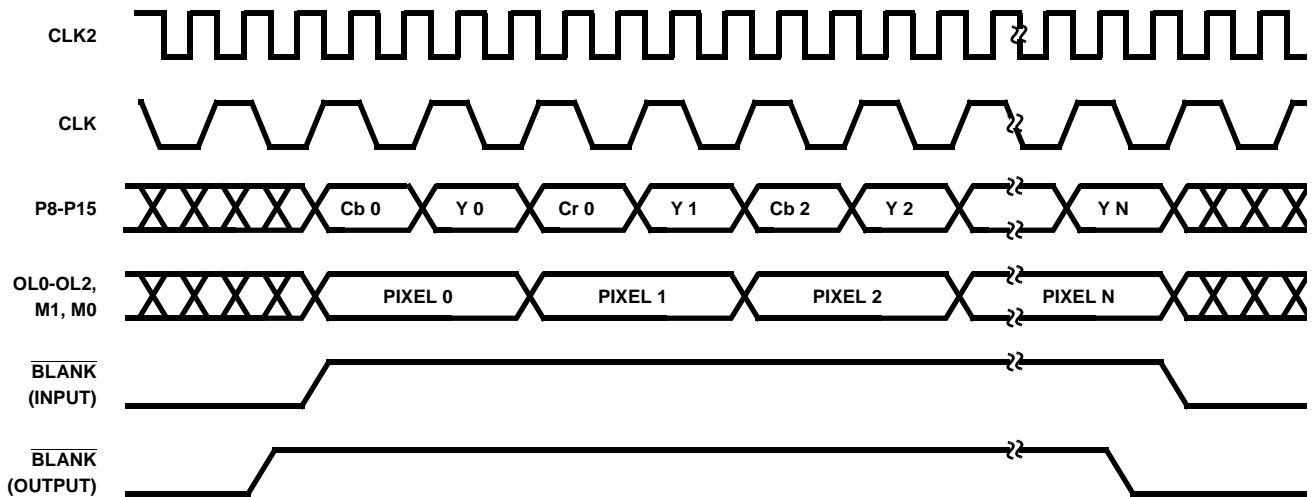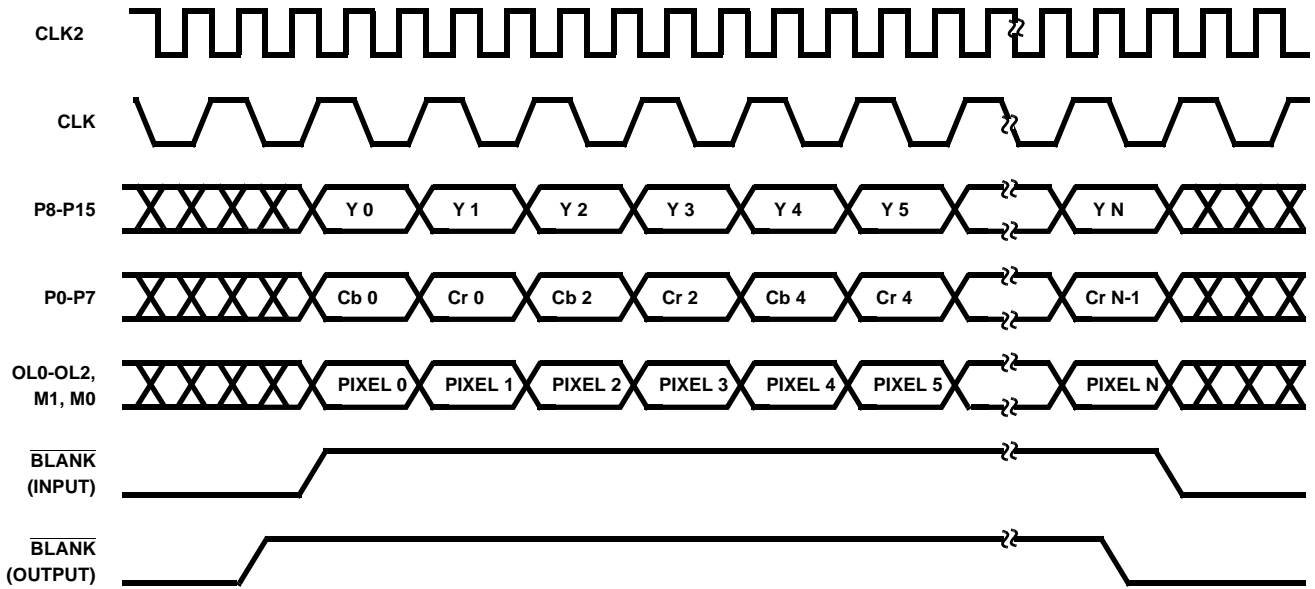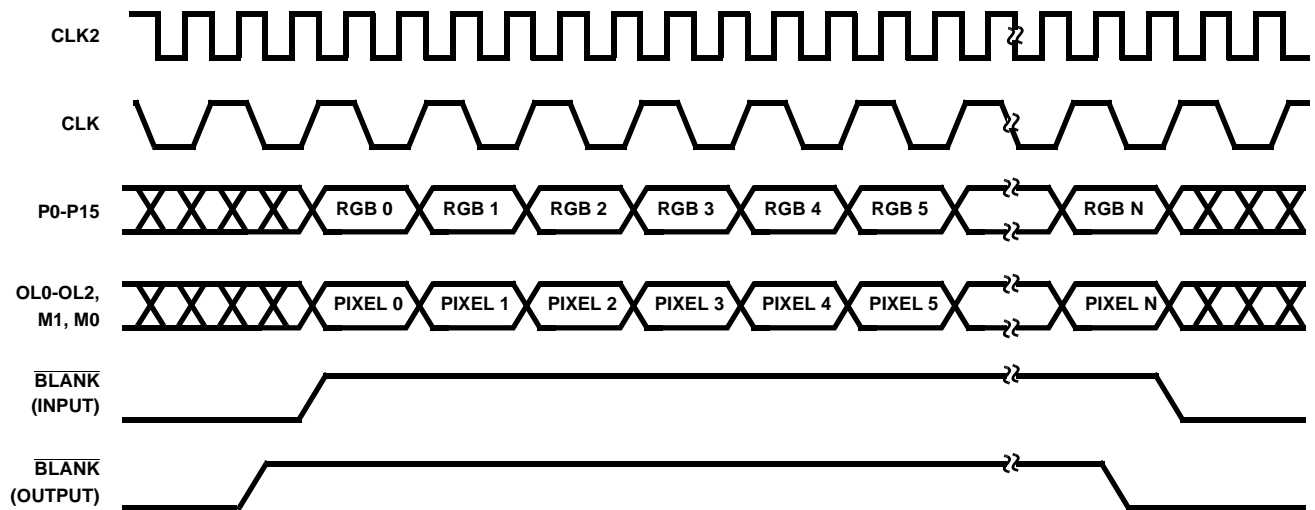**FIGURE 1. PIXEL AND OVERLAY INPUT TIMING - NORMAL 8-BIT YCBCR**

FIGURE 2. PIXEL AND OVERLAY INPUT TIMING - 8-BIT YCBCR WITH 2X UPSCALING

Normal 16-Bit YCbCr, 16-Bit RGB, 24-Bit RGB Formats

When 16-bit YCbCr, 16-bit RGB data, or 24-bit RGB format is selected without 2X upscaling or flicker filtering, the pixel data is latched on the rising edge of CLK2 while CLK is low. Overlay data is also latched on the rising edge of CLK2 while CLK is low. The pixel and overlay input timing is shown in Figures 3 - 5.

As inputs, $\overline{BLANK}$, $\overline{HSYNC}$, and $\overline{VSYNC}$ are latched on the rising edge of CLK2 while CLK is low. As outputs, $\overline{HSYNC}$, $\overline{VSYNC}$, and $\overline{BLANK}$ are output following the rising edge of CLK2 while CLK is high. In these modes of operation, CLK is one-half the CLK2 frequency.

FIGURE 3. PIXEL AND OVERLAY INPUT TIMING - NORMAL 16-BIT YCBCR

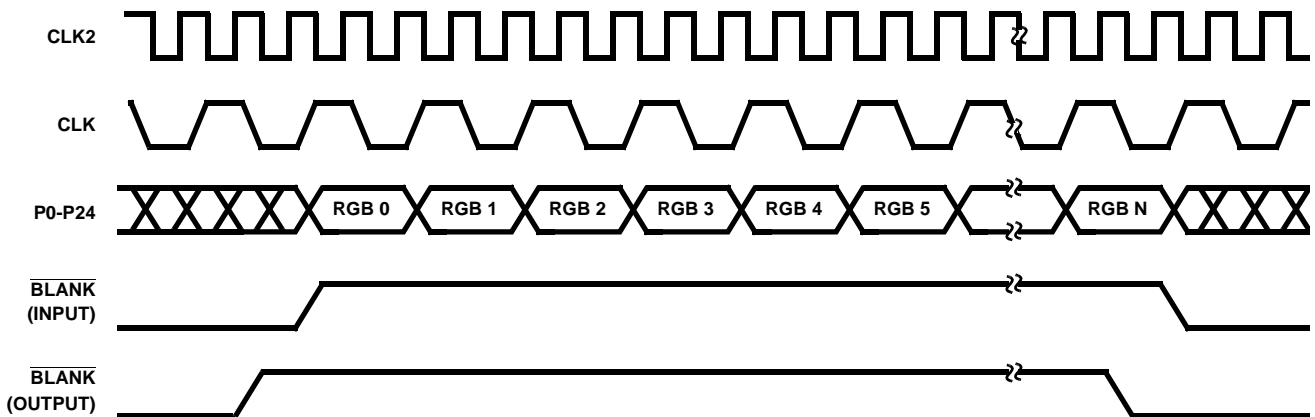**FIGURE 4. PIXEL AND OVERLAY INPUT TIMING - NORMAL 16-BIT RGB**

FIGURE 5. PIXEL AND OVERLAY INPUT TIMING - NORMAL 24-BIT RGB

16-Bit YCbCr, 16-Bit RGB, 24-Bit RGB Formats with 2X Upscaling

When 16-bit YCbCr, 16-bit RGB data, or 24-bit RGB format is selected and 2X upscaling is enabled, data is latched on the rising edge of CLK2 while CLK is low. Overlay data is latched on the rising edge of CLK2 while CLK is low. The pixel and overlay input timing is shown in Figures 6-8.

As inputs, $\overline{BLANK}$, $\overline{HSYNC}$, and $\overline{VSYNC}$ are latched on the rising edge of CLK2 while CLK is low. As outputs, $\overline{HSYNC}$, $\overline{VSYNC}$, and $\overline{BLANK}$ are output following the rising edge of CLK2 while CLK is high. CLK is one-fourth the CLK2 frequency.
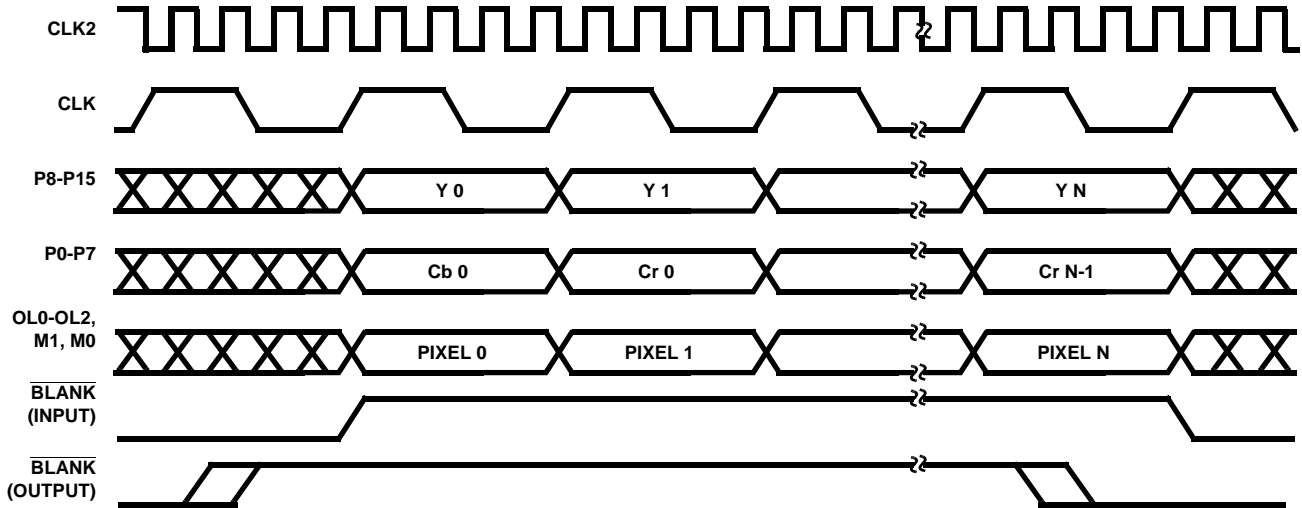

FIGURE 6. PIXEL AND OVERLAY INPUT TIMING - 16-BIT YCBCR WITH 2X UPSAMPLING
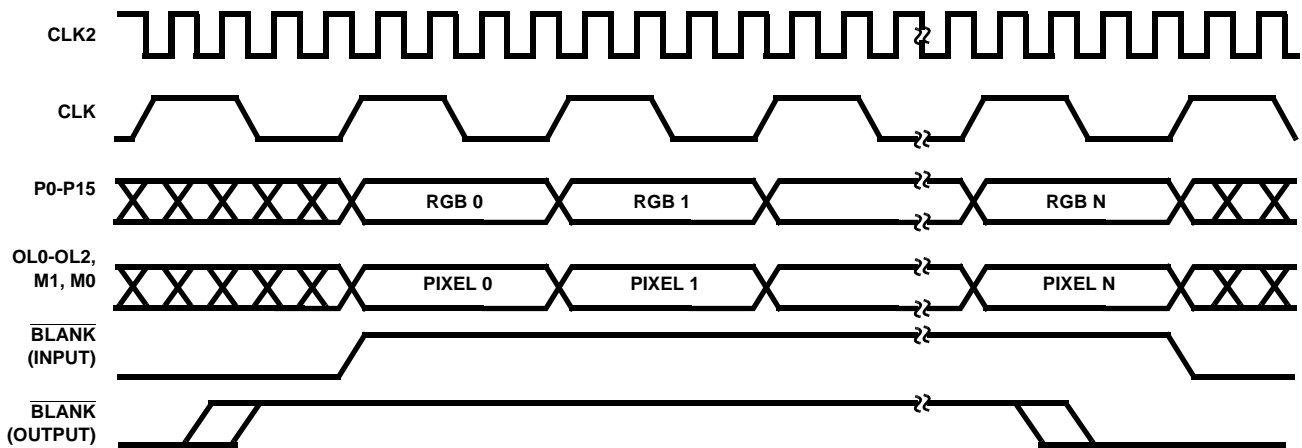

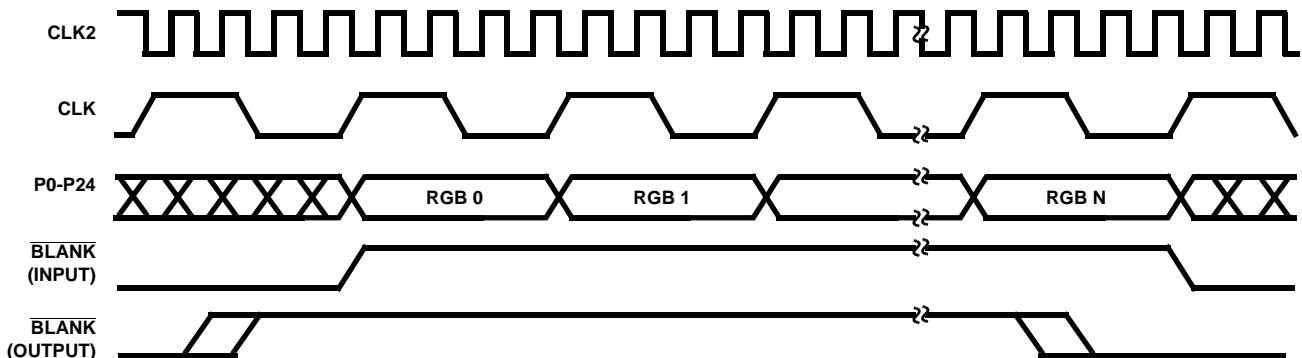**FIGURE 7. PIXEL AND OVERLAY INPUT TIMING - 16-BIT RGB WITH 2X UPSAMPLING**

FIGURE 8. PIXEL AND OVERLAY INPUT TIMING - 24-BIT RGB WITH 2X UPSAMPLING

16-Bit YCbCr, 16-Bit RGB, 24-Bit RGB Formats with Flicker Filtering

When the 16-bit YCbCr, 16-bit RGB, or 24-bit RGB data format is selected and flicker filtering is enabled, pixel and overlay data is latched on every rising edge of CLK2. The pixel and overlay input timing is shown in Figures 9-11.

As inputs, $\overline{BLANK}$, $\overline{HSYNC}$, and $\overline{VSYNC}$ are latched on each rising edge of CLK2. As outputs, $\overline{BLANK}$, $\overline{HSYNC}$, and $\overline{VSYNC}$ are output following the rising edge of CLK2. If the CLK pin is configured as an input, it is ignored. If configured as an output, it is one-half the CLK2 frequency.
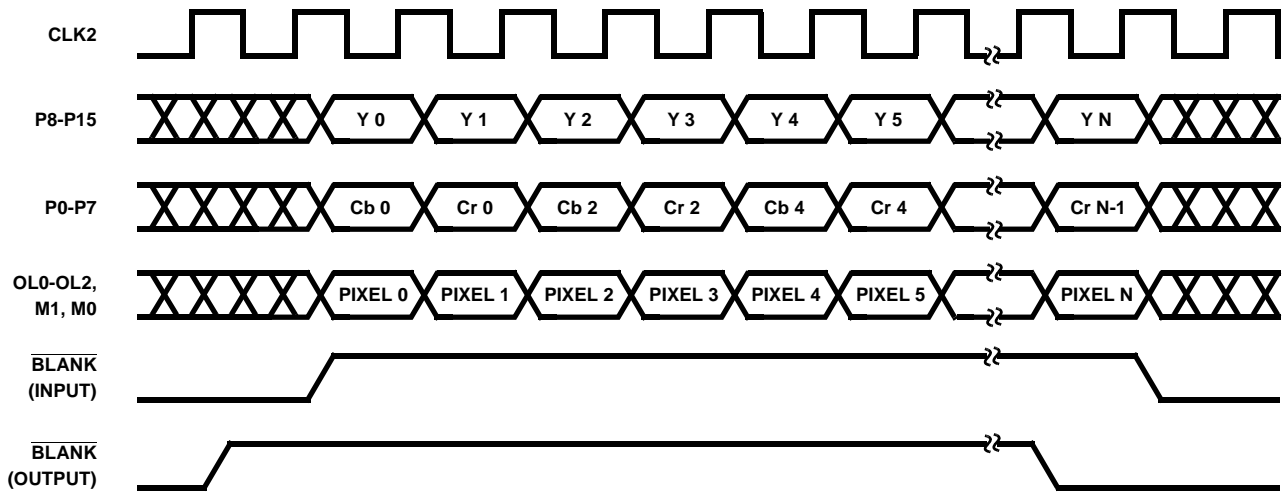
FIGURE 9. PIXEL AND OVERLAY INPUT TIMING - 16-BIT YCBCR WITH FLICKER FILTERING
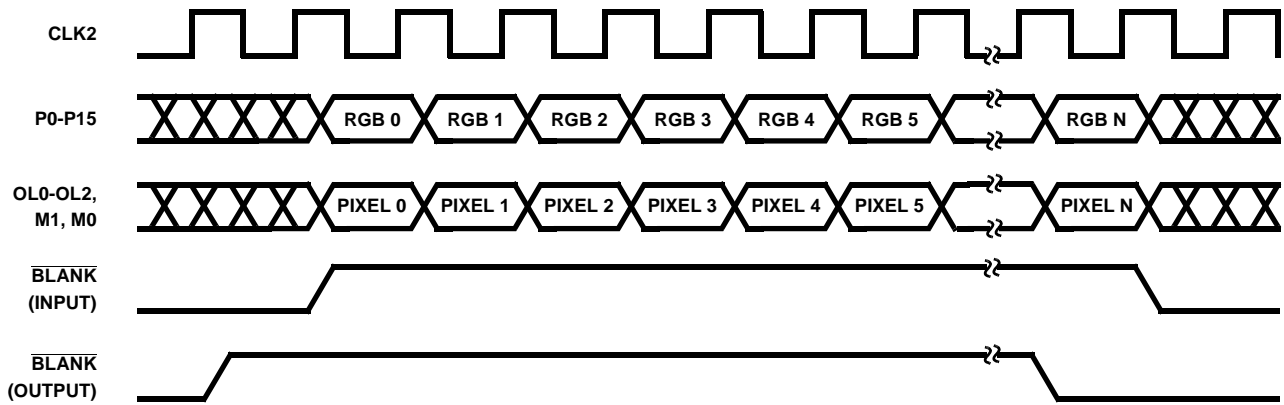
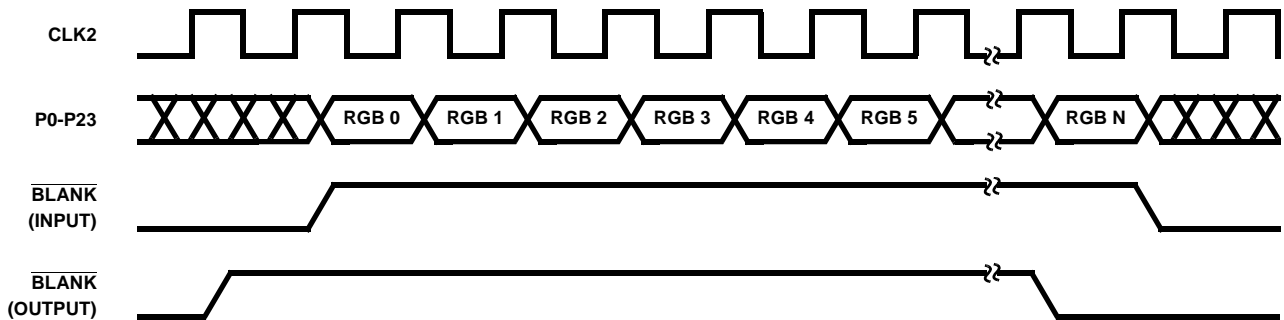FIGURE 10. PIXEL AND OVERLAY INPUT TIMING - 16-BIT RGB WITH FLICKER FILTERING

FIGURE 11. PIXEL AND OVERLAY INPUT TIMING - 24-BIT RGB WITH FLICKER FILTERING
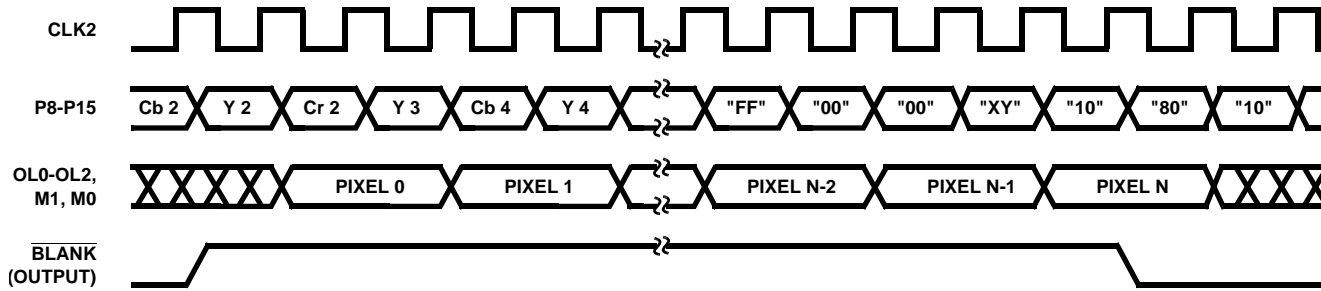
FIGURE 12. PIXEL AND OVERLAY INPUT TIMING - BT.656

8-Bit BT.656 Format

When BT.656 format is selected, data is latched on each rising edge of CLK2. Overlay data is latched when the Y input data is latched. However, the overlay data must arrive three pixels after its corresponding Y data. The pixel and overlay input timing is shown in Figure 12.

As inputs, the $\overline{BLANK}$, $\overline{HSYNC}$, and $\overline{VSYNC}$ pins are ignored since all timing is derived from the EAV and SAV sequences within the data stream. As outputs, $\overline{BLANK}$, $\overline{HSYNC}$ and $\overline{VSYNC}$ are output following the rising edge of CLK2. If the CLK pin is configured as an input, it is ignored. If configured as an output, it is one-half the CLK2 frequency.

Square pixel operation, overlay processing with internal mixing, flicker filtering, and SIF mode 2X upsampling are not supported for the BT.656 input format. Also, the $\overline{HSYNC}$, $\overline{VSYNC}$, and $\overline{BLANK}$ signals must be configured as outputs.

Video Timing Control

Regardless of the input mode, the output video timing of the HMP8154/HMP8156A is at 50 or 59.94 fields per second (interlaced). For normal and 2X upscaling modes, the pixel input timing is at 50 or 59.94 fields per second; with the flicker filter enabled, the input timing rate is twice as fast. The output video and pixel input timing is controlled by the $\overline{BLANK}$, $\overline{HSYNC}$, $\overline{VSYNC}$, FIELD, and CLK2 pins.

HSYNC, VSYNC, and Field Timing

The leading edge of $\overline{HSYNC}$ indicates the beginning of a horizontal sync interval. If $\overline{HSYNC}$ is an output, it is asserted for about 4.7μs. If $\overline{HSYNC}$ is an input, it must be active for at least two CLK2 periods. The width of the horizontal composite sync tip is determined from the video standard and does not depend on the width of $\overline{HSYNC}$.

The leading edge of $\overline{VSYNC}$ indicates the beginning of a vertical sync interval. If $\overline{VSYNC}$ is an output, it is asserted for 3 scan lines in (M, NSM) NTSC and (M, N) PAL modes or 2.5 scan lines in (B, D, G, H, I, CN) PAL modes. If $\overline{VSYNC}$ is an input, it must be asserted for at least two CLK2 periods.

When $\overline{HSYNC}$ and $\overline{VSYNC}$ are configured as outputs, their leading edges will occur simultaneously at the start of an

odd field. At the start of an even field, the leading edge of $\overline{VSYNC}$ occurs in the middle of the line.

When $\overline{HSYNC}$ and $\overline{VSYNC}$ are configured as inputs, the HMP8154/HMP8156A provides a programmable $\overline{HSYNC}$ window for determining FIELD. The window is specified with respect to the leading or trailing edge of $\overline{VSYNC}$. The edge is selected in the field control register. When $\overline{HSYNC}$ is found inside the window, then the encoder sets FIELD to the value specified in the field control register.

The HMP8154/HMP8156A provides programmable timing for the $\overline{VSYNC}$ input. At the active edge of $\overline{VSYNC}$, the encoder resets its vertical half-line counter to the value specified by the field control register. This allows the input and output syncs to be offset, although the data must still be aligned.

The FIELD signal is always an output and changes state near each leading edge of $\overline{VSYNC}$. The delay between the syncs and FIELD depends on the encoder's operating mode as summarized in Table 6. In modes in which the encoder uses CLK to gate its inputs and outputs, the FIELD signal may be delayed 0-12 additional CLK2 periods.

Figure 13 illustrates the $\overline{HSYNC}$, $\overline{VSYNC}$, and FIELD general timing for (M, NSM) NTSC and (M, N) PAL. Figure 14 illustrates the general timing for (B, D, G, H, I, CN) PAL. In the figures, all the signals are shown active low (their reset state), and FIELD is low during odd fields.

TABLE 6. FIELD OUTPUT TIMING

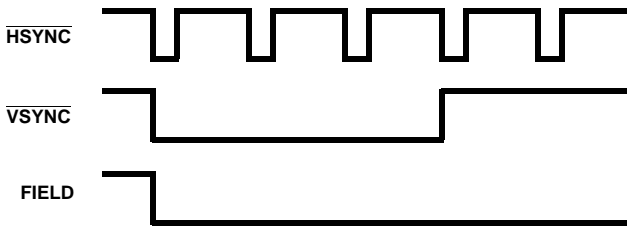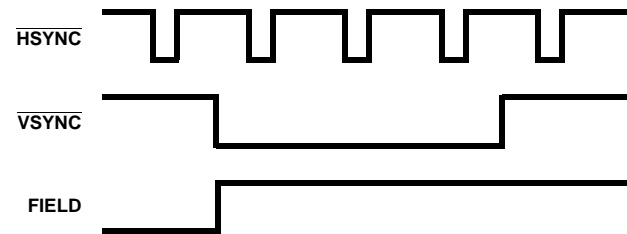| OPERATING MODE			
SYNC I/O DIRECTION	BLANK I/O DIRECTION	CLK2 DELAY	COMMENTS
Input	Input	148	FIELD lags $\overline{VSYNC}$ switching from odd to even. FIELD lags the earlier of $\overline{VSYNC}$ and $\overline{HSYNC}$ when syncs are aligned when switching from even to odd.
Input	Output	138	FIELD lags $\overline{VSYNC}$.
Output	Don't Care	32	FIELD leads $\overline{VSYNC}$.

FIGURE 13A. BEGINNING AN ODD FIELD

FIGURE 13B. BEGINNING AN EVEN FIELD

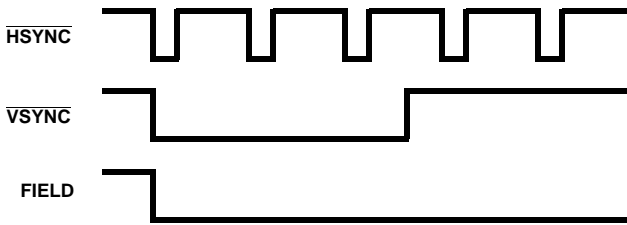FIGURE 13. $\overline{HSYNC}$, $\overline{VSYNC}$, AND FIELD TIMING FOR (M, NSM) NTSC AND (M, N) PAL

FIGURE 14A. BEGINNING AN ODD FIELD

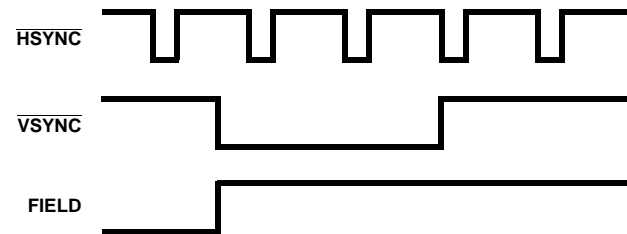FIGURE 14B. BEGINNING AN EVEN FIELD

FIGURE 14. $\overline{HSYNC}$, $\overline{VSYNC}$, AND FIELD TIMING FOR (B, D, G, H, I, CN) PAL

$\overline{BLANK}$ Timing

The encoder uses the $\overline{HSYNC}$, $\overline{VSYNC}$, FIELD signals to generate a standard composite video waveform with no active video (black burst). The signal includes only sync tips, color burst, and optionally, a 7.5 IRE blanking setup. Based on the $\overline{BLANK}$ signal, the encoder adds the pixel and overlay input data to the video waveform.

The encoder ignores the pixel and overlay input data when $\overline{BLANK}$ is asserted. Instead of the input data, the encoder generates the blanking level. The encoder also ignores the pixel and overlay inputs when generating closed captioning data on a specific line, even if $\overline{BLANK}$ is negated.

There must be an even number of active and total pixels per line. In the 8-bit YCbCr modes, the number of active and total pixels per line must be a multiple of four. Note that if $\overline{BLANK}$ is an output, half-line blanking on the output video cannot be done.

The HMP8154/HMP8156A never adds a 7.5 IRE blanking setup during the active line time on scan lines 1-21 and 263-284 for (M, NSM) NTSC, scan lines 523-18 and 260-281 for (M) PAL, and scan lines 623-22 and 311-335 for (N) PAL, allowing the generation of video test signals, timecode, and other information by controlling the pixel inputs appropriately.

Normal Mode Blanking

The relative timing of $\overline{BLANK}$, $\overline{HSYNC}$, and the output video depends on the blanking and sync I/O directions. The typical timing relation is shown in Figure 15. The delays which vary with operating mode are indicated. The width of the composite sync tip and the location and duration of the color burst are fixed based on the video format.
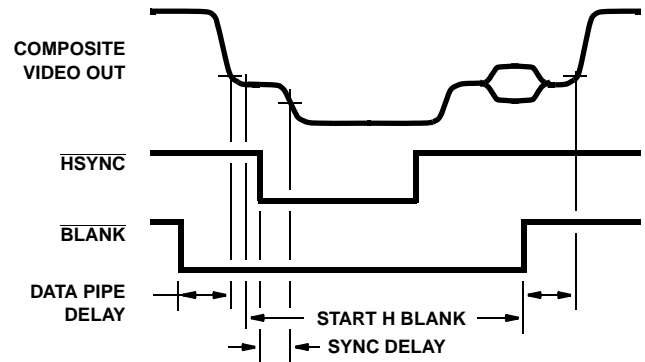
FIGURE 15. $\overline{HSYNC}$, $\overline{BLANK}$, AND OUTPUT VIDEO TIMING, NORMAL MODE

When $\overline{BLANK}$ is an output, the encoder asserts it during the inactive portions of active scan lines (horizontal blanking) and for all of each inactive scan line (vertical blanking). The inactive scan lines blanked each field are determined by the start_v_blank and end_v_blank registers. The inactive portion of active scan lines is determined by the start_h_blank and end_h_blank registers.

The zero count for horizontal blanking is 32 CLK2 cycles before the 50% point of the composite sync. From this zero point, the HMP8154/HMP8156A counts every other CLK2 cycle. When the count reaches the value in the start_h_blank register, the encoder negates $\overline{BLANK}$. When the count reaches the value in the end_h_blank register, $\overline{BLANK}$ is asserted. There may be an additional 0-7 CLK2 delays in modes which use CLK.

The data pipeline delay through the HMP8154/HMP8156A is 26 CLK2 cycles. In operating modes which use CLK to gate the inputs into the encoder, the delay may be an additional 0-7 CLK2 cycles. The delay from $\overline{BLANK}$ to the start or end of active video is an additional one-half CLK cycle when the blank timing select bit is cleared. The active video may also appear to end early or start late since the HMP8154/HMP8156A controls the blanking edge rates.

The delay from the active edge of $\overline{\text{HSYNC}}$ to the 50% point of the composite sync is 4-39 CLK2 cycles depending on the HMP8154/HMP8156A operating mode. The delay is shortest when the encoder is the timing master; it is longest when in slave mode.

Flicker Filter Blanking

When the flicker filter is enabled, $\overline{\text{BLANK}}$ occurs twice per line. However, $\overline{\text{HSYNC}}$ does not change and still matches the horizontal syncs of the composite output. The default timing of $\overline{\text{BLANK}}$ with respect to $\overline{\text{HSYNC}}$ is shown in Figure 16.

FIGURE 16A. BEGINNING AN EVEN FIELD

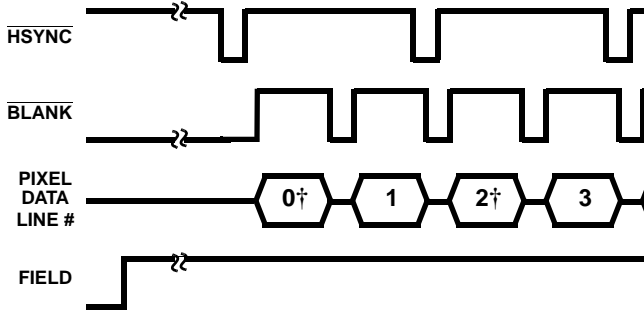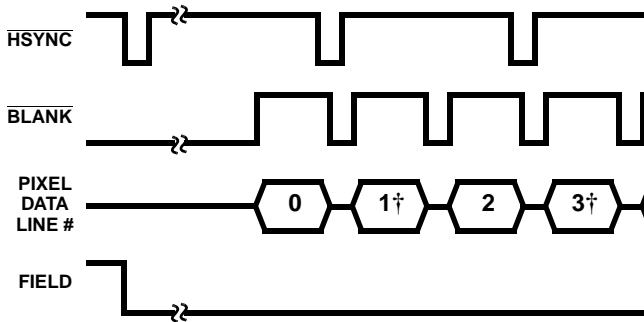

FIGURE 16B. BEGINNING AN ODD FIELD

FIGURE 16. $\overline{\text{HSYNC}}$ AND $\overline{\text{BLANK}}$ TIMING WITH THE FLICKER FILTER ENABLED. $\overline{\text{VSYNC}}$ ALIGNS WITH EITHER EDGE OF FIELD. † UNBLANKED PERIOD WHICH DETERMINES ACTIVE VIDEO IN OUTPUT.

Only the first unblanked period during each line time determines when the active video will be output. Because of the half line offset between the H and V syncs, pixel data input begins (blanking ends) in the middle of the line time for odd fields. However, it is still the unblanked period immediately after $\overline{\text{HSYNC}}$ which generates the active region of the output video. During even fields, the unblanking pulses for the even numbered lines determine the output timing; during odd fields, it's the odd numbered lines.

When it is an output and the flicker filter is enabled, $\overline{\text{BLANK}}$ generation is similar to that found in normal mode. The main difference is that the encoder counts every CLK2 instead of every other CLK2. The start and end times for each line's second unblanked interval are shifted slightly. The unblanked intervals are the same number of pixels but the blanked

intervals are not. The count values for $\overline{\text{BLANK}}$ transitions are shown in Figure 17.
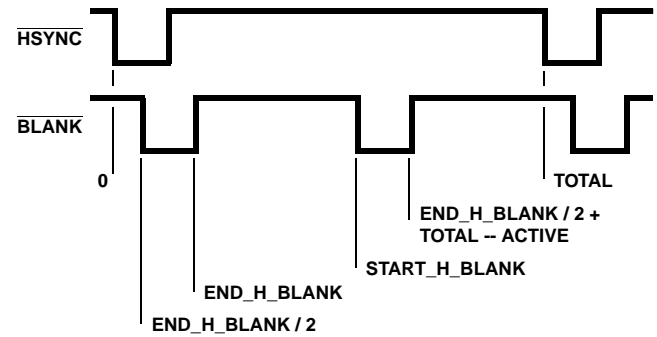

FIGURE 17. FLICKER FILTER $\overline{\text{BLANK}}$ OUTPUT TIMING COUNTS. TOTAL DEPENDS ON FORMAT. ACTIVE = START_H_BLANK -- END_H_BLANK

CLK2 Input Timing

The CLK2 input clocks all of the HMP8154/HMP8156A, including its video timing counters. For proper operation, all of the HMP8154/HMP8156A inputs must be synchronous with CLK2. The frequency of CLK2 depends on the device's operating mode and the total number of pixels per line. The standard clock frequencies are shown in Table 7.

Note that the color subcarrier is derived from the CLK2 input. Any jitter on CLK2 will be transferred to the color subcarrier, resulting in color changes. Just 400ps of jitter on CLK2 causes up to a 1 degree color subcarrier phase shift. Thus, CLK2 should be derived from a stable clock source, such as a crystal. The use of a PLL to generate CLK2 is not recommended.

Video Processing

Upsampling

Video processing begins with the 4:4:4 sampled YCbCr data from the input processor. After overlay mixing and optional 2X upscaling or flicker filtering, the HMP8154/HMP8156A upsamples the 4:4:4 data to generate 8:8:8 data. The encoder uses linear interpolation for the upsampling.

Horizontal Filtering

Unless disabled, the HMP8154/HMP8156A lowpass filters the Y data to 6.0MHz. Lowpass filtering Y removes any aliasing artifacts due to the upsampling process, and simplifies the analog output filters. The Y 6.0MHz lowpass filter response is shown in Figure 18. At this point, the HMP8154/HMP8156A also scales the Y data to generate the proper output levels for the various video standards

The HMP8154/HMP8156A lowpass filters the Cb and Cr data to 1.3MHz prior to modulation. The lowpass filtering removes any aliasing artifacts due to the upsampling process (simplifying the analog output filters) and also properly bandwidth-limits Cb and Cr prior to modulation. The chrominance filtering is not optional like luminance filtering. The Cb and Cr 1.3MHz lowpass filter response is shown in Figure 19.

TABLE 7. TYPICAL VIDEO TIMING PARAMETERS

|	PIXELS PER LINE		HBLANK REGISTER VALUES		VBLANK REGISTER VALUES		CLK2 (MHz)
VIDEO STANDARD	TOTAL	ACTIVE	START	END	START	END	
FULL INPUT RESOLUTION, RECTANGULAR PIXELS							
(M, NSM) NTSC	858	720	842 (0x34a)	122 (0x7a)	259 (0x103)	19 (0x13)	27.0
(B, D, G, H, I) PAL	864	720	853 (0x355)	133 (0x85)	310 (0x136)	22 (0x16)	27.0
(M) PAL	858	720	842 (0x34a)	122 (0x7a)	259 (0x103)	19 (0x13)	27.0
(N) PAL	864	720	853 (0x355)	133 (0x85)	309 (0x135)	21 (0x15)	27.0
(CN) PAL	864	720	853 (0x355)	133 (0x85)	310 (0x136)	22 (0x16)	27.0
FULL INPUT RESOLUTION, SQUARE PIXELS							
(M, NSM) NTSC	780	640	758 (0x2f6)	118 (0x76)	259 (0x103)	19 (0x13)	24.54
(B, D, G, H, I) PAL	944	768	923 (0x39b)	155 (0x9b)	310 (0x136)	22 (0x16)	29.5
(M) PAL	780	640	758 (0x2f6)	118 (0x76)	259 (0x103)	19 (0x13)	24.54
(N) PAL	944	768	923 (0x39b)	155 (0x9b)	309 (0x135)	21 (0x15)	29.5
(CN) PAL	944	768	923 (0x39b)	155 (0x9b)	310 (0x136)	22 (0x16)	29.5
SIF INPUT RESOLUTION, RECTANGULAR PIXELS							
(M, NSM) NTSC	429	352	834 (0x342)	130 (0x82)	259 (0x103)	19 (0x13)	27.0
(B, D, G, H, I) PAL	432	352	845 (0x34d)	141 (0x8d)	310 (0x136)	22 (0x16)	27.0
(M) PAL	429	352	842 (0x34a)	122 (0x7a)	259 (0x103)	19 (0x13)	27.0
(N) PAL	432	352	853 (0x355)	133 (0x85)	309 (0x135)	21 (0x15)	27.0
(CN) PAL	432	352	853 (0x355)	133 (0x85)	310 (0x136)	22 (0x16)	27.0
SIF INPUT RESOLUTION, SQUARE PIXELS							
(M, NSM) NTSC	390	320	758 (0x2f6)	118 (0x76)	259 (0x103)	19 (0x13)	24.54
(B, D, G, H, I) PAL	472	384	923 (0x39b)	155 (0x9b)	310 (0x136)	22 (0x16)	29.5
(M) PAL	390	320	758 (0x2f6)	118 (0x76)	259 (0x103)	19 (0x13)	24.54
(N) PAL	472	384	923 (0x39by)	155 (0x9b)	309 (0x135)	21 (0x15)	29.5
(CN) PAL	472	384	923 (0x39b)	155 (0x9b)	310 (0x136)	22 (0x16)	29.5
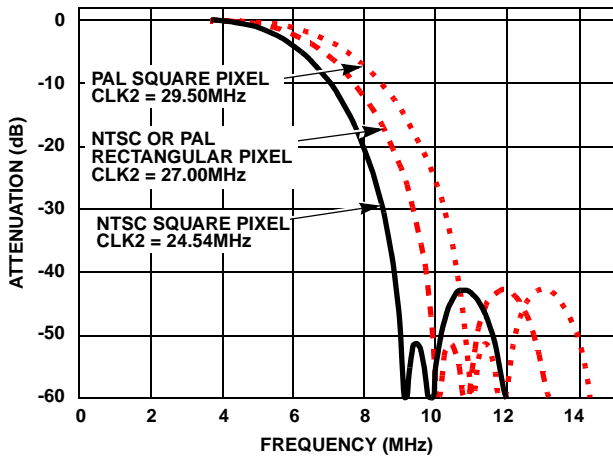
FIGURE 18A. FULL SPECTRUM
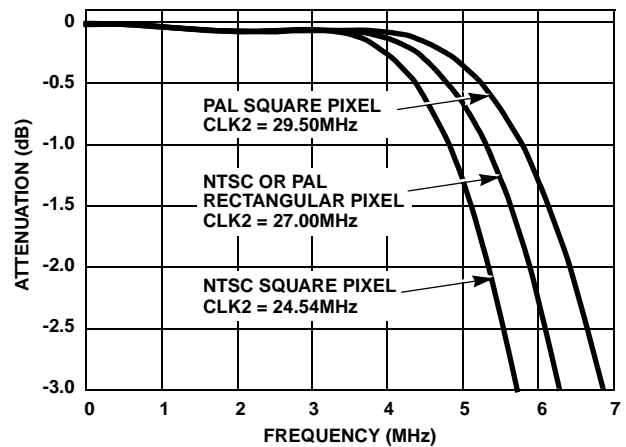
FIGURE 18B. PASS BAND
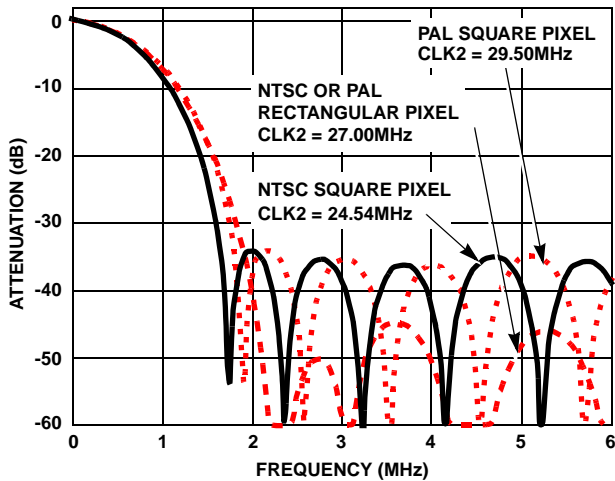
FIGURE 18. Y LOWPASS FILTER RESPONSE
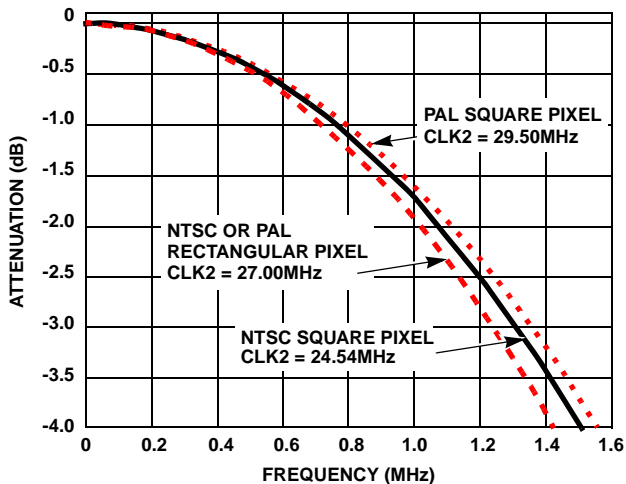
FIGURE 19A. FULL SPECTRUM

FIGURE 19B. PASS BAND
FIGURE 19. Cb AND Cr LOWPASS FILTER RESPONSE

Chrominance Modulation

The HMP8154/HMP8156A uses a numerically controlled oscillator (NCO) clocked by CLK2 and a sine look up ROM to generate the color subcarrier. The subcarrier from the ROM is pre-scaled to generate the proper levels for the various video standards. Prescaling outside the CbCr data path minimizes color processing artifacts. The HMP8154/HMP8156A modulates the filtered 8:8:8 chrominance data with the synthesized subcarrier.

Subcarrier Phase

The SCH phase is 0 degrees after reset but then changes monotonically over time due to residue in the NCO. In an ideal system, zero SCH phase would be maintained forever. In reality, this is impossible to achieve due to pixel clock frequency tolerances.

If enabled, the HMP8154/HMP8156A resets the NCO periodically to avoid an accumulation of SCH phase error. The reset occurs at the beginning of each field to burst phase sequence. The sequence repeats every 4 fields for NTSC or 8 fields for PAL.

Resetting the SCH phase every four fields (NTSC) or eight fields (PAL) avoids the accumulation of SCH phase error at the expense of requiring any NTSC/PAL decoder after the encoder be able to handle very minor "jumps" (up to 2°) in the SCH phase at the beginning of each four-field or eight-field sequence. Most NTSC/PAL decoders are able to handle this due to video editing requirements.

Composite Video Limiting

The HMP8154/HMP8156A adds the luminance and modulated chrominance together with the sync, color burst, and optional blanking pedestal to form the composite video data. If enabled in the video processing register, the encoder limits the active video so that it is always greater than one-eighth of full scale. This corresponds to approximately one-half the sync height. This allows the generation of "safe" video in the event nonstandard YCbCr values are input to the device.

Closed Captioning

If enabled in the auxiliary data control register, the HMP8154/HMP8156A generates closed captioning data on specified scan lines. The captioning data stream includes clock run-in and start bits followed by the captioning data. During closed captioning encoding, the pixel and overlay inputs are ignored on the scan lines containing captioning information.

The HMP8154/HMP8156A has two 16-bit registers containing the captioning information. Each 16-bit register is organized as two cascaded 8-bit registers. One 16-bit register (caption 21) is read out serially during line 18, 21 or 22; the other 16-bit register (caption 284) is read out serially during line 281, 284 or 335. The data registers are shifted out LSB first.

The bytes may be written in any order but both must be written within one frame time for proper operation. If the registers are not updated, the encoder resends the previously loaded values.

The HMP8154/HMP8156A provides a write status bit for each captioning line. The encoder clears the write status bit to '0' when captioning is enabled and both bytes of the captioning data register have been written. The encoder sets the write status bit to '1' after it outputs the data, indicating the registers are ready to receive new data.

Captioning information may be enabled for either line, both lines, or no lines. The captioning modes are summarized in Table 8.

Controlled Edges

The NTSC and PAL video standards specify edge rates and rise and fall times for portions of the video waveform. The HMP8154/HMP8156A automatically implements controlled edge rates and rise and fall times on these edges:

1. Analog horizontal sync (rising and falling edges)
2. Analog vertical sync interval (rising and falling edges)
3. Color burst envelope
4. Blanking of analog active video
5. Overlay with internal mixing
6. Closed captioning information

TABLE 8. CLOSED CAPTIONING MODES

CLOSED CAPTIONING ENABLE BITS	OUTPUT LINE(S)	CAPTIONING REGISTER		WRITE STATUS BIT	
		284A 284B	21A 21B	284	21
00	None	Ignored	Ignored	Always 1	Always 1
01	21 (NTSC) 18 (M PAL) 22 (Other PAL)	Ignored	Caption Data	Always 1	0 = Loaded 1 = Output
10	284 (NTSC) 281 (M PAL) 335 (Other PAL)	Caption Data	Ignored	0 = Loaded 1 = Output	Always 1
11	21, 284 (NTSC) 18, 281 (M PAL) 22, 335 (Other PAL)	Caption Data	Caption Data	0 = Loaded 1 = Output	0 = Loaded 1 = Output

Analog Outputs

The HMP8154/HMP8156A converts the video data into analog signals using four 10-bit DACs running at the CLK2 rate. The DACs output a current proportional to the digital data. The full scale output current is determined by the reference voltage VREF and an external resistor RSET. The full scale output current is given by:

$$I_{FULLSCALE} \text{ (mA)} = 3.9 * VREF \text{ (V)} / RSET \text{ (k}\Omega\text{)} \quad \text{(EQ 1.)}$$

VREF must be chosen such that it is within the part's operating range; RSET must be chosen such that the maximum output current is not exceeded.

If the VREF pin is not connected, the HMP8154/HMP8156A provides an internal reference voltage. Otherwise, the applied voltage overdrives the internal reference. If an external reference is used, it must decoupled from any power supply noise. An example external reference circuit is shown in the Applications section.

The HMP8154/HMP8156A generates $1V_{P-P}$ nominal video signals across 37.5Ω loads corresponding to doubly terminated 75Ω lines. The encoder may also drive larger loads. The full scale output current and load must be chosen such that the maximum output voltage is not exceeded.

Output DAC Filtering

Since the DACs run at 2X the pixel sample rate, the sin(x)/x rolloff of the outputs is greatly reduced, and there are fewer high frequency artifacts in the output spectrum. This allows using simple analog output filters. The analog output filter should be flat to $F_S/4$ and have good rejection at $3F_S/4$. Example filters are shown in the Applications section.

Composite + Y/C Output Mode

The HMP8154/HMP8156A provides three output modes: S-video, RGB, and power down. When S-video outputs are selected, the encoder outputs the luminance, modulated chrominance, and two copies of the composite video signals. All four outputs are time aligned.

Composite + RGB Output Mode

When analog RGB video is selected, the HMP8154/HMP8156A transforms the filtered 8:8:8 YCbCr data into 8:8:8 RGB data. The transform matrix uses different coefficients to generate NTSC or PAL video levels.

The analog RGB outputs have a range of 0.3-1.0V with an optional blanking pedestal. Composite sync information (0.0-0.3V) may be optionally added to the green output. Closed captioning data is not included on the RGB outputs. The HMP8154/HMP8156A also generates composite video when in RGB output mode. All four outputs are time aligned.

The HMP8154/HMP8156A provides selectable pin outs for the RGB outputs. When the SCART compatibility bit is cleared, the analog composite video is output onto the NTSC/PAL 1 pin. Red information is output onto the NTSC/PAL 2 pin, blue information is output onto the C pin, and green information is output onto the Y pin.

When the bit is set, the analog composite video is output onto the Y pin. Red information is output onto the C pin, blue video is output on the NTSC/PAL 2 pin, and the green signal is output on the NTSC/PAL 1 pin. The output pin assignments are summarized in Table 9.

TABLE 9. OUTPUT PIN ASSIGNMENTS

PIN NAME	PIN #	OUTPUT MODE (SCART SELECT BIT)		
		COMP. WITH Y/C (X)	COMP. W/ RGB (0)	COMP. W/ RGB (1)
Y	3	Luma	Green	Composite
C	7	Chroma	Blue	Red
NTSC/PAL 1	11	Composite	Composite	Green
NTSC/PAL 2	15	Composite	Red	Blue

Power Down Modes

To reduce power dissipation, any of the four output DACs may be turned off. Each DAC has an independent enable bit. Each output may be disabled in the host control register.

When the power down mode is enabled, all of the DACs and internal voltage reference are powered down (forcing their outputs to zero) and the data pipeline registers are disabled. The host processor may still read from and write to the internal control registers.

Host Interfaces

Reset

The HMP8154/HMP8156A resets to its default operating mode on power up, when the reset pin is asserted for at least four CLK cycles, or when the software reset bit of the host control register is set. During the reset cycle, the encoder returns its internal registers to their reset state and deactivates the I^{2}C interface.

I^{2}C Interface

The HMP8154/HMP8156A provides a standard I^{2}C interface and supports fast-mode (up to 400 Kbps) transfers. The device acts as a slave for receiving and transmitting data only. It will not respond to general calls or initiate a transfer. The encoder's slave address is either 0100 000x$_B$ when the SA input pin is low or 0100 001x$_B$ when it is high. (The 'x' bit in the address is the I^{2}C read flag.)

The I^{2}C interface consists of the SDA and SCL pins. When the interface is not active, SCL and SDA must be pulled high using external 4-6kΩ pull-up resistors. The I^{2}C clock and data timing is shown in Figures 20 and 21.

During I^{2}C write cycles, the first data byte after the slave address specifies the sub address, and is written into the address register. Only the seven LSBs of the subaddress are used; the MSB is ignored. Any remaining data bytes in the I^{2}C write cycle are written to the control registers, beginning with the register specified by the address register. The 7-bit address register is incremented after each data byte in the I^{2}C write cycle. Data written to reserved bits within registers or reserved registers is ignored.

During I^{2}C read cycles, data from the control register specified by the address register is output. The address register is incremented after each data byte in the I^{2}C read cycle. Reserved bits within registers return a value of "0". Reserved registers return a value of 00$_H$.

The HMP8154/HMP8156A's operating modes are determined by the contents of its internal registers which are accessed via the I^{2}C interface. All internal registers may be written or read by the host processor at any time. However, some of the bits and words are read only or reserved and data written to these bits is ignored.

Table 10 lists the HMP8154/HMP8156A's internal registers. Their bit descriptions are listed in Tables 11-30.

TABLE 10. CONTROL REGISTER NAMES

SUB ADDRESS (HEX)	CONTROL REGISTER	RESET CONDITION
00	Product ID	54$_H$
01	Output Format	00$_H$
02	Input Format	06$_H$
03	Video Processing	A0$_H$
04	Timing I/O 1	00$_H$
05	Timing I/O 2	00$_H$
06	Aux Data Enable	00$_H$
07-0E	Reserved	-
0F	Host Control	0C$_H$
10	Closed Caption_21A	80$_H$
11	Closed Caption_21B	80$_H$
12	Closed Caption_284A	80$_H$
13	Closed Caption_284B	80$_H$
14-1F	Reserved	-
20	Start H_Blank Low	4A$_H$
21	Start H_Blank High	03$_H$
22	End H_Blank	7A$_H$
23	Start V_Blank Low	03$_H$
24	Start V_Blank High	01$_H$
25	End V_Blank	13$_H$
26	Field Control 1	80H
27	Field Control 2	00H
28-2F	Reserved	-
30-7F	Test and Unused	-
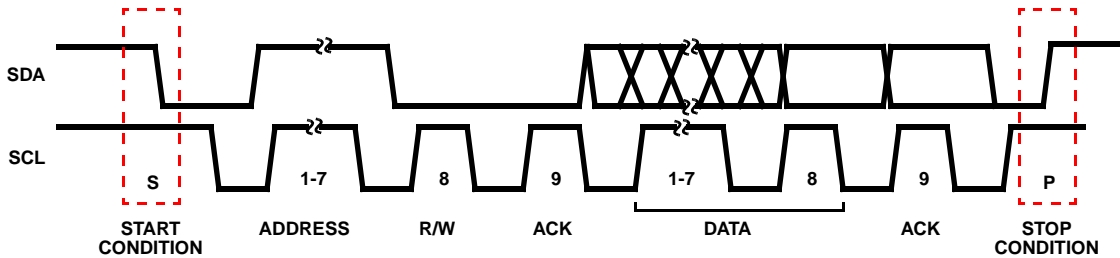
FIGURE 20. I^{2}C SERIAL TIMING FLOW
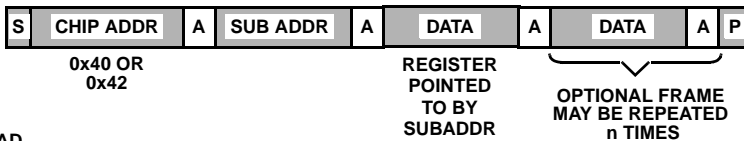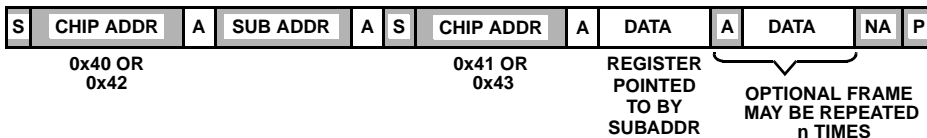
FIGURE 21. REGISTER WRITE PROGRAMMING FLOW

TABLE 11. PRODUCT ID REGISTER

		SUB ADDRESS = 00$_H$	
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Product ID	This 8-bit register specifies the last two digits of the product number. It is a read-only register. Data written to it is ignored.	54$_H$

TABLE 12. OUTPUT FORMAT REGISTER

		SUB ADDRESS = 01$_H$	
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-5	Video Timing Standard	000 = (M) NTSC 001 = (M) NTSC with a 0 IRE setup; also called (NSM) NTSC 010 = (B, D, G, H, I) PAL 011 = (M) PAL 100 = (N) PAL 101 = combination (N) PAL; also called (CN) PAL 110 = reserved 111 = reserved	000$_B$
4-3	Output Format	00 = Composite + Y/C 01 = reserved 10 = Composite + RGB (no sync on green) 11 = Composite + RGB (with sync on green)	00$_B$
2-0	Reserved		000$_B$

TABLE 13. INPUT FORMAT REGISTER

		SUB ADDRESS = 02$_H$	
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-5	Input Format	000 = 16-bit 4:2:2 YCbCr 001 = 8-bit 4:2:2 YCbCr 010 = 8-bit BT.656 011 = 16-bit linear RGB 100 = 16-bit gamma-corrected RGB 101 = 24-bit linear RGB 110 = 24-bit gamma-corrected RGB 111 = Blue screen	000$_B$
4	Gamma Select	These bits are ignored except during linear RGB input modes. 0 = 1 / 2.2 1 = 1 / 2.8	0$_B$
3	Reserved		0$_B$
2-1	Overlay Mixing Mode	These bits must be set to "11" in 24-bit RGB input modes. Internal mixing should not be selected in BT.656 input mode. 00 = No mixing 01 = Internal mixing 10 = External mixing 11 = Disable overlays	11$_B$
0	Input Resolution	This bit must be set to "0" during BT.656 input mode and when the flicker filter is enabled. 0 = Full resolution (2X upscaling disabled) 1 = SIF resolution (2X upscaling enabled)	0$_B$

TABLE 14. VIDEO PROCESSING REGISTER

SUB ADDRESS = 03_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	Luminance Processing	0 = None 1 = Y Lowpass filtering enabled	1_B
6	Composite Video Limiting	0 = None 1 = Lower limit of composite active video is about half the sync height	0_B
5	SCH Phase Mode	0 = Never reset SCH phase 1 = Reset SCH phase every 4 (NTSC) or 8 (PAL) fields	1_B
4	RGB Pedestal Enable	0 = Don't add blanking pedestal to RGB output 1 = add blanking pedestal to RGB output	0_B
3	RGB pin Assignment select	0 = use HMP8156 assignments 1 = SCART connector compatible	0_B
2	First Active Line Select	This bit is ignored unless flicker filtering is enabled. This bit is ignored on the HMP8156. 0 = First line of active video in odd fields is on an odd line number 1 = First line of active video in odd fields is on an even line number	0_B
1-0	Flicker Filter Processing	These bits must be "00" during 8-bit YCbCr and BT.656 input modes, and SIF input resolution mode. These bits are always "00" on the HMP8156A. 00 = No flicker filtering 01 = reserved 10 = reserved 11 = 3-line flicker filtering enabled	00_B

TABLE 15. TIMING I/O REGISTER #1

SUB ADDRESS = 04_H			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	$\overline{BLANK}$ Timing Select	This bit is ignored unless $\overline{BLANK}$ is configured to be an output. 0 = Data for the first active pixel of the scan line must arrive the CLK cycle after the encoder negates $\overline{BLANK}$. 1 = Data for the first active pixel of the scan line must arrive immediately after the encoder negates $\overline{BLANK}$.	0_B
6	Reserved		0_B
5	$\overline{BLANK}$ Output Control	0 = $\overline{BLANK}$ is an input 1 = $\overline{BLANK}$ is an output	0_B
4	$\overline{BLANK}$ Polarity	0 = Active low (low during blanking) 1 = Active high (high during blanking)	0_B
3	$\overline{HSYNC}$ and $\overline{VSYNC}$ Output Control	0 = $\overline{HSYNC}$ and $\overline{VSYNC}$ are inputs 1 = $\overline{HSYNC}$ and $\overline{VSYNC}$ are outputs	0_B
2	$\overline{HSYNC}$ Polarity	0 = Active low (low during horizontal sync) 1 = Active high (high during horizontal sync)	0_B
1	$\overline{VSYNC}$ Polarity	0 = Active low (low during vertical sync) 1 = Active high (high during vertical sync)	0_B
0	FIELD Polarity	0 = Active low (low during odd fields) 1 = Active high (high during odd fields)	0_B

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TABLE 16. TIMING I/O REGISTER #2

		SUB ADDRESS = 05$_H$	
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-5	Reserved		000$_B$
4	CLK Output Control	0 = CLK is an input 1 = CLK is an output	0$_B$
3	Aspect Ratio Mode	This bit must be set to "0" during BT.656 input mode. 0 = Rectangular (BT.601) pixels 1 = Square pixels	0$_B$
2-0	Reserved		00$_B$

TABLE 17. AUXILIARY DATA ENABLE REGISTER

		SUB ADDRESS = 06$_H$	
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-6	Closed Captioning Enable	00 = Closed caption disabled 01 = Closed caption enabled for odd fields: line 21 for NTSC, line 18 for (M) PAL, or line 22 for (B, D, G, H, I, N, CN) PAL 10 = Closed caption enabled for even fields: line 284 for NTSC, line 281 for (M) PAL, or line 335 for (B, D, G, H, I, N, CN) PAL 11 = Closed caption enabled for both odd and even fields	00$_B$
5-0	Reserved		000000$_B$

TABLE 18. HOST CONTROL REGISTER

		SUB ADDRESS = 0F$_H$	
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7	Software Reset	Setting this bit to "1" initiates a software reset. It is automatically reset to a "0" after the reset sequence is complete.	0$_B$
6	Power Down Enable	0 = Normal operation 1 = Power down mode	0$_B$
5	NTSC/PAL 2 Output Mode	0 = Enabled 1 = Disabled	0$_B$
4	Closed Caption Line 21 Write Status	0 = Caption_21A and Caption_21B data registers contain unused data 1 = Data has been output, host processor may now write to the registers	1$_B$
3	Closed Caption Line 284 Write Status	0 = Caption_284A and Caption_284B data registers contain unused data 1 = Data has been output, host processor may now write to the registers	1$_B$
2	NTSC/PAL 1 Output Mode	0 = Enabled 1 = Disabled	0$_B$
1	Y/G Output Mode	0 = Enabled 1 = Disabled	0$_B$
0	C/B Output Mode	0 = Enabled 1 = Disabled	0$_B$

TABLE 19. CLOSED CAPTION_21A DATA REGISTER

SUB ADDRESS = 10$_H$			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Line 21 Caption Data (First Byte)	This register is cascaded with the closed caption_21B data register and they are read out serially as 16 bits during line 18, 21, or 22 if line 21 captioning is enabled. Bit D0 of the 21A data register is shifted out first.	80$_H$

TABLE 20. CLOSED CAPTION_21B DATA REGISTER

SUB ADDRESS = 11$_H$			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Line 21 Caption Data (Second Byte)	This register is cascaded with the closed caption_21A data register and they are read out serially as 16 bits during line 18, 21, or 22 if line 21 captioning is enabled. Bit D0 of the 21A data register is shifted out first.	80$_H$

TABLE 21. CLOSED CAPTION_284A DATA REGISTER

SUB ADDRESS = 12$_H$			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Line 284 Caption Data (First Byte)	This register is cascaded with the closed caption_284B data register and they are read out serially as 16 bits during line 281, 284, or 335 if line 284 captioning is enabled. Bit D0 of the 284A data register is shifted out first.	80$_H$

TABLE 22. CLOSED CAPTION_284B DATA REGISTER

SUB ADDRESS = 13$_H$			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Line 284 Caption Data (Second Byte)	This register is cascaded with the closed caption_284A data register and they are read out serially as 16 bits during line 281, 284, or 335 if line 284 captioning is enabled. Bit D0 of the 284A data register is shifted out first.	80$_H$

TABLE 23. START H_BLANK LOW REGISTER

SUB ADDRESS = 20$_H$			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Assert $\overline{BLANK}$ Output Signal (Horizontal)	This 8-bit register is cascaded with Start H_Blank High Register to form a 10-bit start_horizontal_blank register. It specifies the horizontal count (in 1X clock cycles) at which to start ignoring pixel data each scan line. The leading edge of $\overline{HSYNC}$ is count 020$_H$. This register is ignored unless $\overline{BLANK}$ is configured as an output.	4A$_H$

TABLE 24. START H_BLANK HIGH REGISTER

SUB ADDRESS = 21$_H$			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-2	Reserved		000000$_B$
1-0	Assert $\overline{BLANK}$ Output Signal (Horizontal)	This 2-bit register is cascaded with Start H_Blank Low Register to form a 10-bit start_horizontal_blank register. It specifies the horizontal count (in 1x clock cycles) at which to start ignoring pixel data each scan line. The leading edge of $\overline{HSYNC}$ is count 020$_H$. This register is ignored unless $\overline{BLANK}$ is configured as an output.	11$_B$

TABLE 25. END H_BLANK REGISTER

SUB ADDRESS = 22$_H$			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Negate $\overline{BLANK}$ Output Signal (Horizontal)	This 8-bit register specifies the horizontal count (in 1X clock cycles) at which to start inputting pixel data each scan line. The leading edge of $\overline{HSYNC}$ is count 000$_H$. This register is ignored unless $\overline{BLANK}$ is configured as an output.	7A$_H$

TABLE 26. START V_BLANK LOW REGISTER

SUB ADDRESS = 23$_H$			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Assert $\overline{BLANK}$ Output Signal (Vertical)	This 8-bit register is cascaded with Start V_Blank High Register to form a 9-bit start_vertical_blank register. During normal operation, it specifies the line number (n) to start ignoring pixel input data (and what line number to start blanking the output video) each odd field; for even fields, it occurs on line (n + 262) or (n + 313). During SIF input mode, the register value (n) specifies the line number to start ignoring pixel input data each noninterlaced input frame. The output video will be blanked starting on line number (n) each odd field; for even fields, it occurs on line (n + 262) or (n + 313). The leading edge of $\overline{VSYNC}$ at the start of an odd field is count 000$_H$ (note that this does not follow standard NTSC or PAL line numbering). This register is ignored unless $\overline{BLANK}$ is configured as an output.	03$_H$

TABLE 27. START V_BLANK HIGH REGISTER

SUB ADDRESS = 24$_H$			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-1	Reserved		0000000$_B$
0	Assert $\overline{BLANK}$ Output Signal (Vertical)	This 1-bit register is cascaded with Start V_Blank Low Register to form a 9-bit start_vertical_blank register. This register is ignored unless $\overline{BLANK}$ is configured as an output.	1$_B$

TABLE 28. END V_BLANK REGISTER

SUB ADDRESS = 25$_H$			
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-0	Negate $\overline{BLANK}$ Output Signal (Vertical)	During normal operation, this 8-bit register specifies the line number (n) to start inputting pixel input data (and what line number to start generating active output video) each odd field; for even fields, it occurs on line (n + 262) or (n + 313). During SIF input mode, the register value (n) specifies the line number to start inputting pixel input data each noninterlaced input frame. The output video will be active starting on line number (n) each odd field; for even fields, it occurs on line (n + 262) or (n + 313). The leading edge of $\overline{VSYNC}$ at the start of an odd field is count 000$_H$ (note that this does not follow standard NTSC or PAL line numbering). This register is ignored unless $\overline{BLANK}$ is configured as an output.	13$_H$

TABLE 29. FIELD CONTROL REGISTER 1

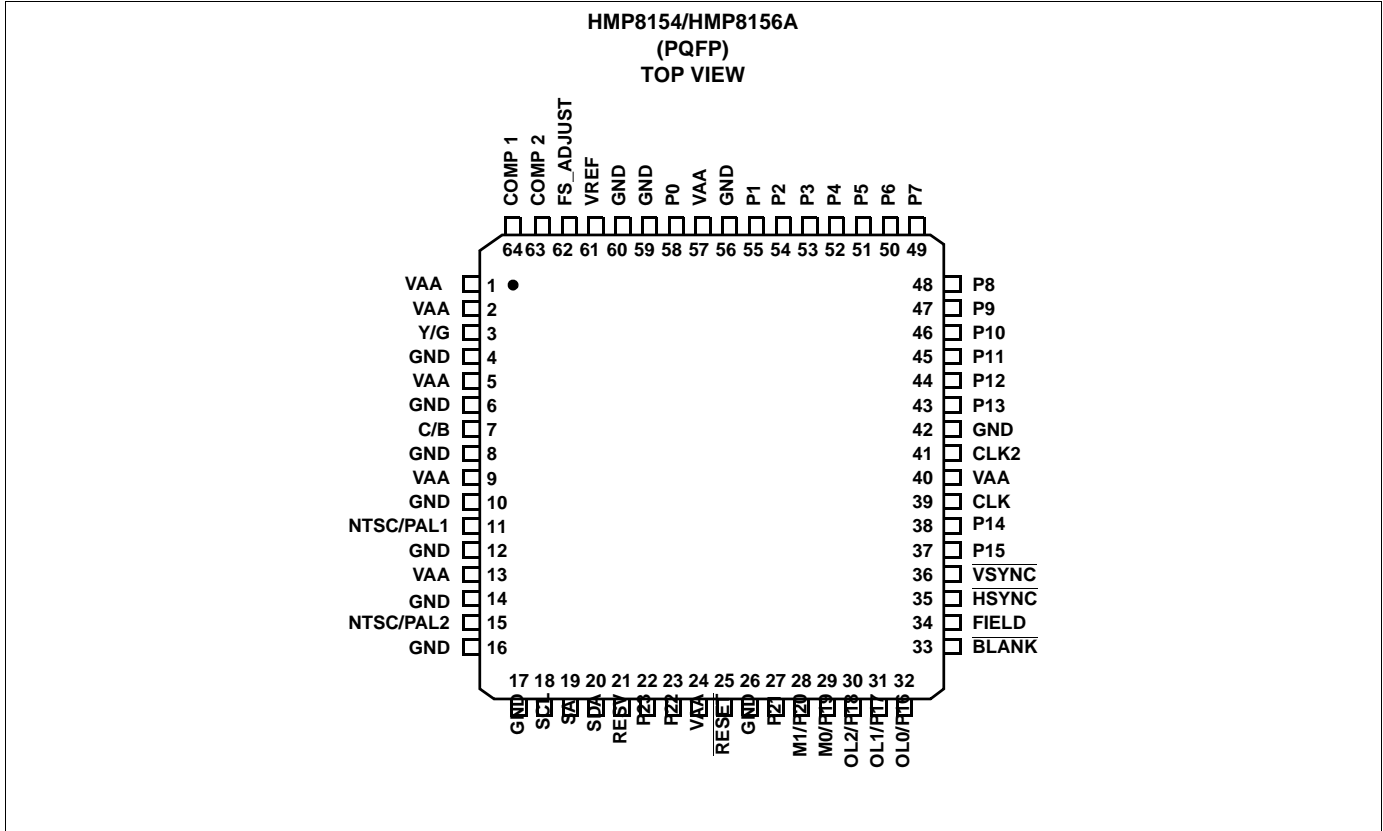| SUB ADDRESS = 26$_H$ |
|---|---|---|---|
| **BIT NUMBER** | **FUNCTION** | **DESCRIPTION** | **RESET STATE** |
| 7-0 | Field Detect Window Size Low | This 8-bit register is cascaded with Field Detect Window Size High to form a 9-bit Field Detect Window Size value. The value specifies the number of 1X clock cycles in the detection window before and after the selected edge of $\overline{VSYNC}$. It may range from 0 to 511. If the leading edge of $\overline{HSYNC}$ occurs within the window, it is the start of an odd or even field, as specified by the FIELD Detect Select bit. This register is ignored unless $\overline{HSYNC}$ and $\overline{VSYNC}$ are configured as inputs. | 80$_H$ |

TABLE 30. FIELD CONTROL REGISTER 2

SUB ADDRESS = 27$_H$
BIT NUMBER	**FUNCTION**	**DESCRIPTION**	**RESET STATE**
7-4	Half Line Count Reset Value	These bits specify the value to load to the vertical half line counter when the selected edge of $\overline{VSYNC}$. The value is ignored when $\overline{HSYNC}$ and $\overline{VSYNC}$ are configured as outputs.	00000$_B$
2	$\overline{VSYNC}$ Edge Select	This bit specifies whether the encoder uses the leading or trailing edge of $\overline{VSYNC}$ to determine the field and to reset the half line counter. It is ignored unless $\overline{HSYNC}$ and $\overline{VSYNC}$ are configured as inputs. 0 = leading edge 1 = trailing edge	0$_B$
1	FIELD Detect Select	This bit specifies whether an odd or even field is starting when the leading edge of $\overline{HSYNC}$ occurs within the FIELD Detect Window. It is ignored unless $\overline{HSYNC}$ and $\overline{VSYNC}$ are configured as inputs. 0 = odd field 1 = even field	0$_B$
0	Field Detect Window Size High	This bit is cascaded with Field Detect Window Size Low to form a 9-bit Field Detect Window Size value. This bit is ignored unless $\overline{HSYNC}$ and $\overline{VSYNC}$ are configured as inputs.	0$_B$

Pinout

HMP8154/HMP8156A
(PQFP)
TOP VIEW

Top pins (64-49): COMP 1, COMP 2, FS_ADJUST, VREF, GND, GND, P0, VAA, GND, P1, P2, P3, P4, P5, P6, P7

Left side pins (1-16):

Pin	Name
1	VAA
2	VAA
3	Y/G
4	GND
5	VAA
6	GND
7	C/B
8	GND
9	VAA
10	GND
11	NTSC/PAL1
12	GND
13	VAA
14	GND
15	NTSC/PAL2
16	GND

Right side pins (48-33):

Pin	Name
48	P8
47	P9
46	P10
45	P11
44	P12
43	P13
42	GND
41	CLK2
40	VAA
39	CLK
38	P14
37	P15
36	$\overline{VSYNC}$
35	$\overline{HSYNC}$
34	FIELD
33	$\overline{BLANK}$

Bottom pins (17-32): GND, SCL, STE, SDA, RESV, P23, P22, VAA, RESET, GND, P21, M1/P20, M0/P19, OL2/P18, OL1/P17, OL0/P16

Pin Descriptions

PIN NAME	PIN NUMBER	INPUT/ OUTPUT	DESCRIPTION
P0-P15	58, 55-43, 38, 37	I	Pixel input pins. See Table 1. Any pixel inputs not used should be connected to GND.
P16-P23	32-27, 23, 22	I	Overlay or pixel inputs. See Table 1. Any overlay or pixel inputs not used should be connected to GND.
RESV	21	I	This pin is reserved and should be connected to VCC or GND.
FIELD	34	O	FIELD output. The field output indicates that the encoder is outputting the odd or even video field. The polarity of FIELD is programmable.
$\overline{HSYNC}$	35	I/O	Horizontal sync input/output. As an input, this pin must be asserted during the horizontal sync intervals. If it occurs early, the line time will be shortened. If it occurs late, the line time will be lengthened by holding the outputs at the front porch level. As an output, it is asserted during the horizontal sync intervals. The polarity of $\overline{HSYNC}$ is programmable. If not driven, the circuit for this pin should include a 4-12kΩ pull up resistor connected to VAA.
$\overline{VSYNC}$	36	I/O	Vertical sync input/output. As an input, this pin must be asserted during the vertical sync intervals. If it occurs early, the field time will be shortened. If it occurs late, the field time will be lengthened by holding the outputs at the blanking level. As an output, it is asserted during the vertical sync intervals. The polarity of $\overline{VSYNC}$ is programmable. If not driven, the circuit for this pin should include a 4-12kΩ pull up resistor connected to VAA.
$\overline{BLANK}$	33	I/O	Composite blanking input/output. As an input, this pin must be asserted during the horizontal and vertical blanking intervals. As an output, it is asserted during the horizontal and vertical blanking intervals. The polarity of $\overline{BLANK}$ is programmable. If not driven, the circuit for this pin should include a 4-12kΩ pull up resistor connected to VAA.

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Pin Descriptions (Continued)

PIN NAME	PIN NUMBER	INPUT/ OUTPUT	DESCRIPTION
CLK	39	I/O	1X pixel clock input/output. As an input, this clock must be free-running and synchronous to the clock signal on the CLK2 pin. As an output, this pin may drive a maximum of one LS TTL load. CLK is generated by dividing CLK2 by two or four, depending on the mode. If not driven, the circuit for this pin should include a 4-12kΩ pull up resistor connected to VAA.
CLK2	41	I	2X pixel clock input. This clock must be a continuous, free-running clock.
SCL	18	I	I^{2}C interface clock input. The circuit for this pin should include a 4-6kΩ pull up resistor connected to VAA.
SA	19	I	I^{2}C interface address select input.
SDA	20	I/O	I^{2}C interface data input/output. The circuit for this pin should include a 4-6kΩ pull-up resistor connected to VAA.
$\overline{\text{RESET}}$	25	I	Reset control input. A logical zero for a minimum of four CLK cycles resets the device. $\overline{\text{RESET}}$ must be a logical one for normal operation.
Y (G)	3	O	Luminance analog current output. This output contains luminance video, sync, blanking, and closed captioning information. In analog RGB output mode, green or composite analog video is generated. It is capable of driving a 37.5Ω load. If not used, it should be connected to GND.
C (B)	7	O	Chrominance analog current output. This output contains chrominance video, and blanking information. In analog RGB output mode, blue or red analog video is generated. It is capable of driving a 37.5Ω load. If not used, it should be connected to GND.
NTSC/PAL 1	11	O	Composite video analog current output. This output contains composite video, sync, blanking, and closed captioning information. In analog RGB output mode, composite or green analog video is generated. It is capable of driving a 37.5Ω load. If not used, it should be connected to GND.
NTSC/PAL 2 (R)	15	O	Composite video analog current output. This output contains composite video, sync, blanking, and closed captioning information. In analog RGB output mode, red or blue analog video is generated. It is capable of driving a 37.5Ω load. If not used, it should be connected to GND.
VREF	61	I/O	Voltage reference. An optional external 1.235V reference may be used to drive this pin. If left floating, the internal voltage reference is used.
FS_ADJUST	62		Full scale adjust control. A resistor (RSET) connected between this pin and GND sets the full-scale output current of each of the DACs.
COMP 1	64		Compensation pin. A 0.1μF ceramic chip capacitor should be connected between this pin and VAA, as close to the device as possible.
COMP 2	63		Compensation pin. Connection to this pin is optional. A 0.1μF ceramic chip capacitor may be connected between this pin and VAA. If used, the capacitor should be placed as close to the device as possible.
VAA			+5V power. A 0.1μF ceramic capacitor, in parallel with a 0.01μF chip capacitor, should be used between each group of VAA pins and GND. These should be as close to the device as possible.
GND			Ground

Absolute Maximum Ratings

V_{AA} . . . .+6V
All Signal Pins . . . . -0.5V to +6V

Operating Conditions

Temperature Range . . . . 0°C to 70°C

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} ^{o}C/W
  PQFP Package.   50
Maximum Junction Temperature . . . . .150°C
Maximum Storage Temperature Range. . . . . -65°C to 150°C
Vapor Phase Soldering, 1 Minute . . . . .220°C
  (PQFP - Lead Tips Only)

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications V_{AA} = +5V ±5%, RSET = 133Ω, VREF Unconnected, T_A = 25°C, Unless Otherwise Specified

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
DC PARAMETERS, DIGITAL INPUTS EXCEPT CLK2, SDA, SCL					
Input Logic Low Voltage, V_{IL}		-	-	0.8	V
Input Logic High Voltage, V_{IH}		2.0	-	-	V
Input Logic Low Current, I_{IL}	V_{IN} = 0V	-	-	-10	μA
Input Logic High Current, I_{IH}	V_{IN} = V_{AA}	-	-	10	μA
Input Capacitance, C_{IN}		-	8	-	pF
DC PARAMETERS, CLK2 INPUT					
Input Logic Low Voltage, V_{IL}		-	-	0.3 x V_{AA}	V
Input Logic High Voltage, V_{IH}		0.7 x V_{AA}	-	-	V
Input Logic Low Current, I_{IL}	V_{IN} = 0V	-	-	-10	μA
Input Logic High Current, I_{IH}	V_{IN} = V_{AA}	-	-	10	μA
Input Capacitance, C_{IN}		-	8	-	pF
DC PARAMETERS, SDA AND SCL INPUTS					
Input Logic Low Voltage, V_{IL}		-	-	0.3 x V_{AA}	V
Input Logic High Voltage, V_{IH}		0.7 x V_{AA}	-	-	V
Input Logic Low Current, I_{IL}	V_{IN} = 0V	-	-	-10	μA
Input Logic High Current, I_{IH}	V_{IN} = V_{AA}	-	-	10	μA
Input Capacitance, C_{IN}		-	8	-	pF
DC PARAMETERS, DIGITAL OUTPUTS (Except SDA)					
Output Logic Low Voltage, V_{OL}	I_{OL} = 2mA	-	-	0.4	V
Output Logic High Voltage, V_{OH}	I_{OH} = -2mA	2.4	-	-	V
Output Capacitance, C_{OUT}		-	8	-	pF
DC PARAMETERS, SDA OUTPUTS					
Output Logic Low Voltage, V_{OL}	I_{OL} = 3mA	-	-	0.4	V
DC PARAMETERS, ANALOG OUTPUTS					
DAC Resolution		10	10	10	Bits
Integral Nonlinearity, INL		-	±0.5	±2.0	LSB
Differential Nonlinearity, DNL		-	±0.2	±1.0	LSB
Output Current		-	-	34.8	mA
Output Impedance	I_{OUT} = 0mA	-	2M	-	Ω
	I_{OUT} = 34mA	-	300K	-	Ω
Output Capacitance	I_{OUT} = 0mA, CLK = 13.5MHz	-	25	-	pF

Electrical Specifications V_{AA} = +5V ±5%, RSET = 133Ω, VREF Unconnected, T_A = 25°C, Unless Otherwise Specified   **(Continued)**

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Output Compliance Range		0	-	1.4	V
Video Level Error	(Note 4)				
Internal Voltage Reference	VREF unconnected, RSET = 133Ω	-	-	±10	%
External Voltage Reference	VREF = 1.230V (Figure 37), RSET = 140Ω	-	-	±10	%
DAC to DAC Matching		-	-	5	%
VREF Output Voltage	Pin not driven, using internal reference	1.13	1.195	1.32	V
VREF Output Current		-50	-	50	μA
VREF Input Voltage	Pin connected to external reference shown in Figure 37.	1.112	1.230	1.358	V
VREF Input Current		-500	-	500	μA
AC PARAMETERS, ANALOG OUTPUTS					
Differential Gain Error	Using analog output filter shown in Figure 38A.	-	1	-	%
Differential Phase Error		-	1	-	Degree
SNR (Weighted)		-	70	-	dB
Hue Accuracy		-	2	-	Degree
Color Saturation Accuracy		-	2	-	%
Luminance Nonlinearity		-	1	-	%
Residual Subcarrier		-	-60	-	dB
SCH Phase	SCH Phase Reset enabled	-	±1.5	-	Degree
Analog Output Skew, T_{ASK}		-	-	3	ns
Analog Output Delay, T_{AD}		-	-	12	ns
DAC-DAC Crosstalk		-	-60	-	dB
Glitch Energy	Using analog output filter shown in Figure 38A. Includes clock and data feedthrough	-	35	-	pV-s
AC PARAMETERS, DIGITAL INPUTS AND OUTPUTS EXCEPT SCL AND SDA					
Setup Time, T_S		8	-	-	ns
Hold Time, T_H		0	-	-	ns
CLK2 Frequency		-	-	30.0	MHz
CLK2 High Time, $CLK2_H$		13.6	-	20.3	ns
CLK2 Low Time, $CLK2_L$		13.6	-	20.3	ns
CLK2 to Output Delay, T_D		2	-	12	ns
RESET* Pulse Width Low, T_{RES}		4	-	-	CLK Cycles
AC PARAMETERS, SCL AND SDA (I^{2}C INTERFACE)					
All AC parameters meet the fast-mode I^{2}C Bus Interface specification.					
POWER SUPPLY CHARACTERISTICS					
DAC PSRR at DC	Note 6	-	64	-	dB
Power Supply Range, V_{AA}		4.75	5.0	5.25	V
Normal Supply Current, I_{AA}		-	-	260	mA
Power-Down Supply Current, I_{AA}	Note 5	-	-	750	μA
Power Dissipation		-	1100	1300	mW

NOTES:

4. Output level is dependent on the voltage on VREF, the value of RSET, and the load.

5. If using an external voltage reference, it is not powered down. The internal voltage reference is always powered down.

6. The supply voltage rejection is the relative variation of the full-scale output driving a 37.5Ω load for a ±0.5% supply variation:
   PSRR = 20 x log ($\Delta V_{AA}/\Delta V_{OUT}$).

Typical Performance Curves

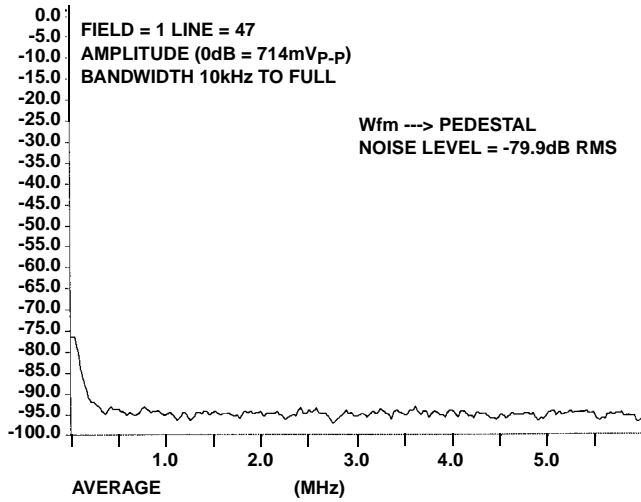FIELD = 1 LINE = 47
AMPLITUDE (0dB = 714mV$_{P-P}$)
BANDWIDTH 10kHz TO FULL

Wfm ---> PEDESTAL
NOISE LEVEL = -79.9dB RMS

AVERAGE   (MHz)

FIGURE 22. NOISE SPECTRUM (NTSC)

APL = 44.3%

SYSTEM LINE L 47 F1
ANGLE (DEG) 0.0
GAIN x1.000
          0.000dB
525 LINE NTSC
BURST FROM SOURCE

SETUP 7.5%
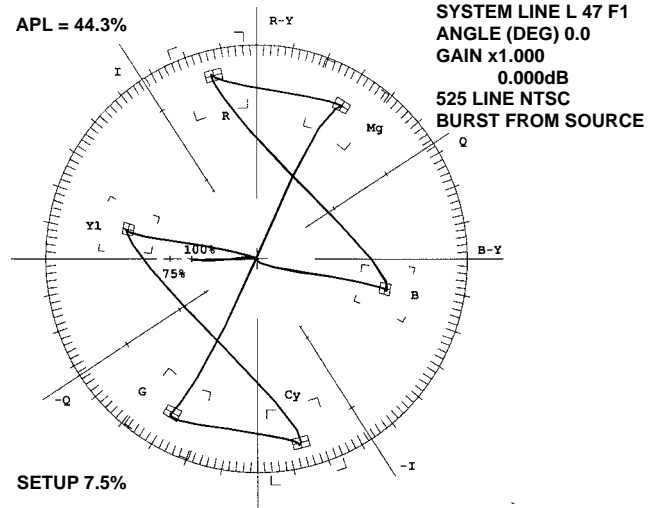
FIGURE 23. NTSC COLOR BAR VECTOR SCOPE

ColorBar (NTSC)
Field = 1 Line = 47
Luminance Level (IRE)

| 79.3 | 71.0 | 57.2 | 48.8 | 36.0 | 27.6 | 14.1 | 5.8 |

Wfm --> FCC Color Bar

Chrominance Level (IRE)

| 0.0 | 63.1 | 88.9 | 83.5 | 82.6 | 89.1 | 63.4 | 0.0 |

Chrominance Phase (deg)

| ------- | 167.1 | 283.1 | 240.5 | 60.6 | 103.6 | 346.6 | ------- |

Gray   Yellow   Cyan   Green   Magenta   Red   Blue   Black

Average
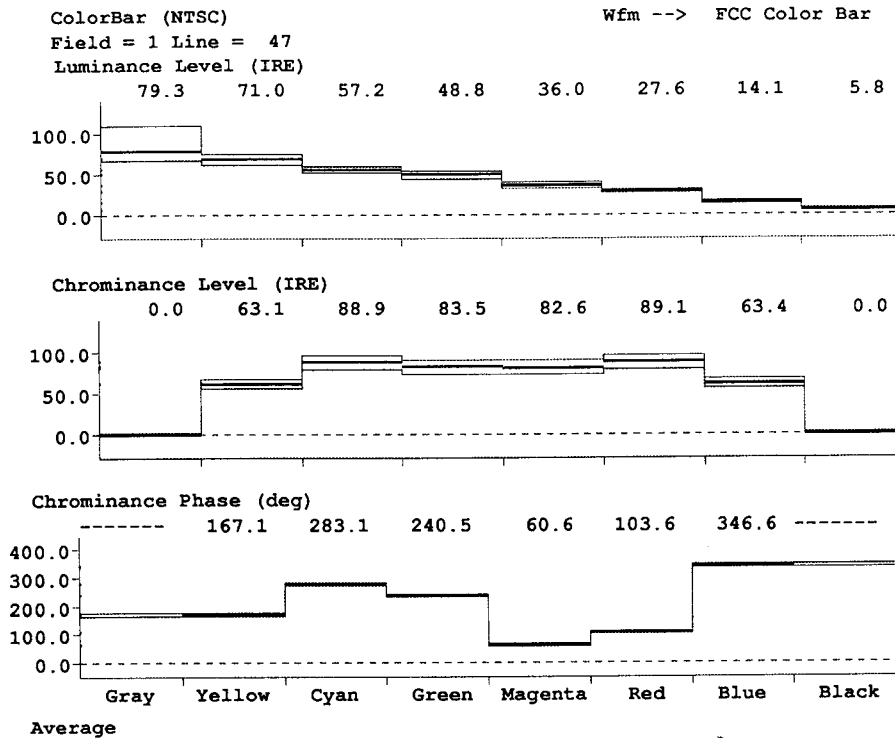
FIGURE 24. NTSC FCC COLOR BAR

intersil

Typical Performance Curves (Continued)
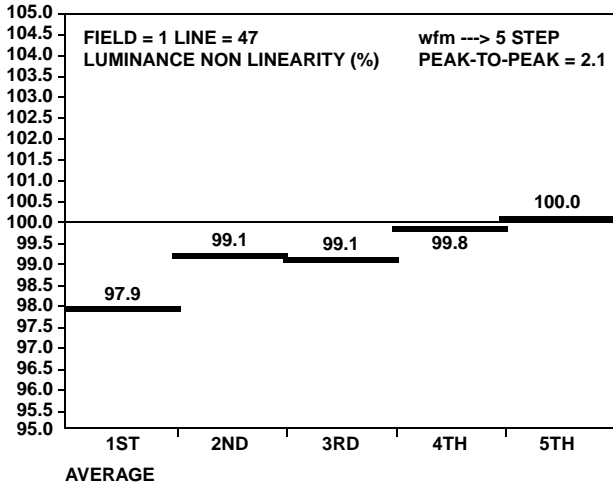
FIGURE 25. LUMINANCE NON LINEARITY (NTSC)
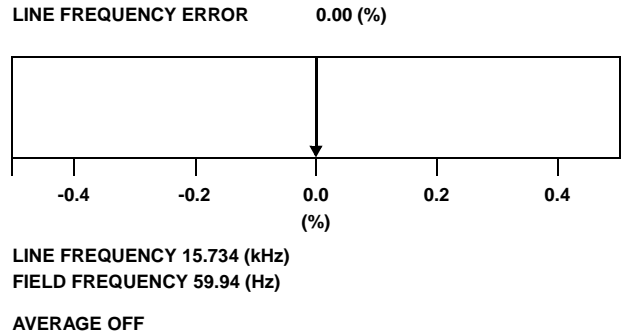
FIGURE 26. LINE FREQUENCY (NTSC)
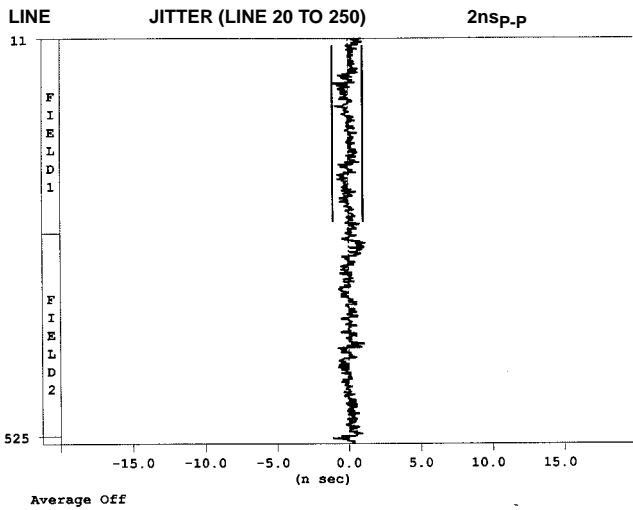
FIGURE 27. H SYNC JITTER IN A FRAME (NTSC)
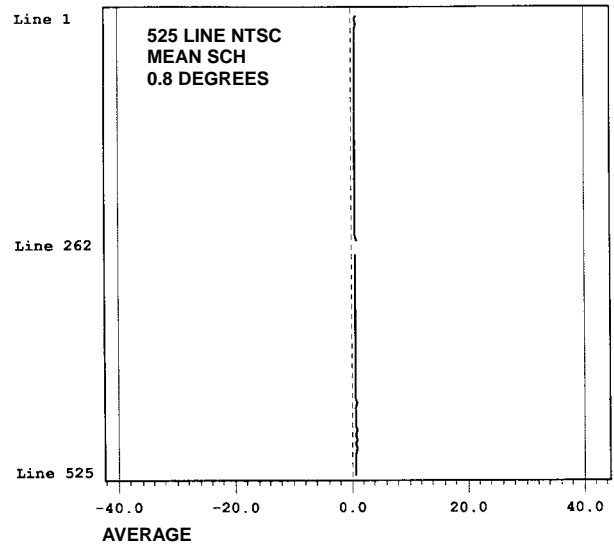
FIGURE 28. SCH PHASE MEASUREMENT (NTSC)
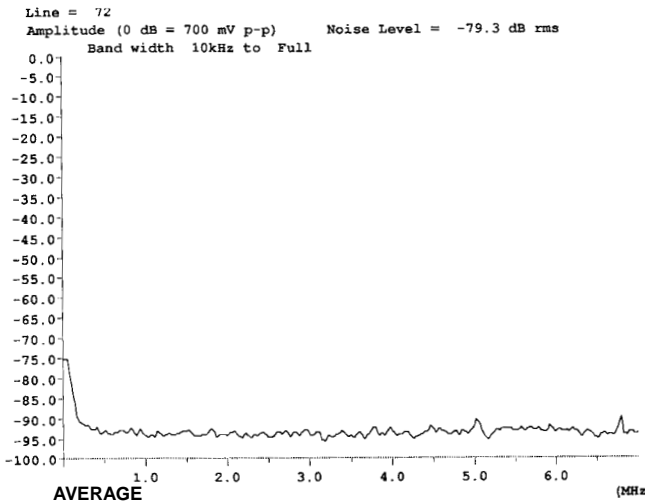
FIGURE 29. NOISE SPECTRUM (PAL)
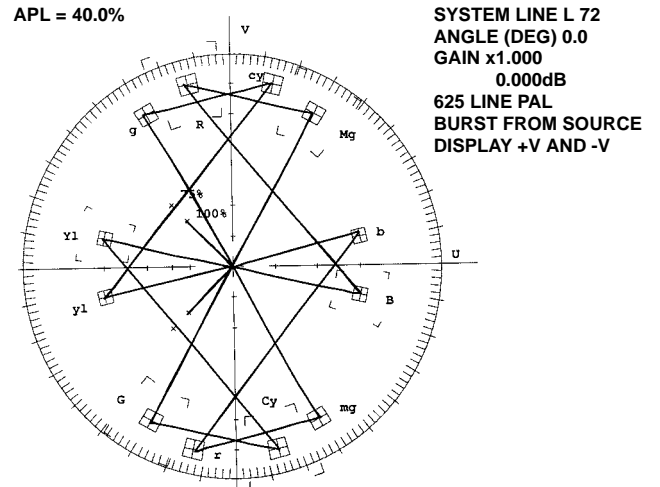
FIGURE 30. PAL COLOR BAR VECTOR SCOPE

Typical Performance Curves (Continued)

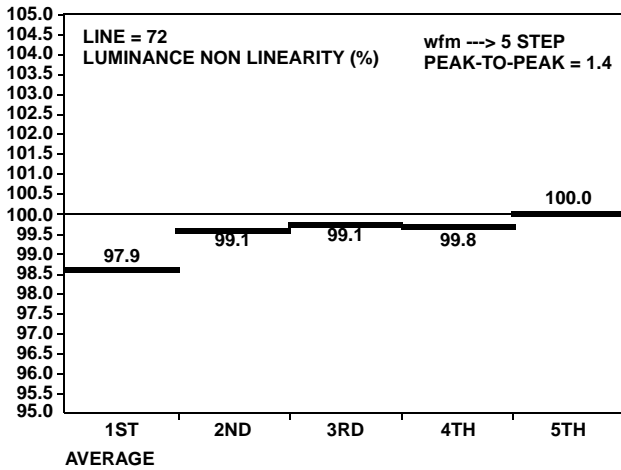LINE = 72   Wfm ---> COLOR BAR
Luminance Level (mV)
        557.2   494.3   390.4   326.5   229.9   165.8   61.1   0.1
1000.0
 500.0
   0.0

Chrominance Level (mV)
          0.2   471.7   666.8   624.9   617.6   667.1   474.4   0.2
1000.0
 500.0
   0.0

Chrominance Phase (deg)
        ------- 167.2   283.6   240.5   60.5   103.5   346.5 -------
400.0
300.0
200.0
100.0
  0.0
         Gray   Yellow   Cyan   Green   Magenta   Red   Blue   Black

Average 32 -> 32

FIGURE 31. COLORBAR (PAL)

LINE = 72
LUMINANCE NON LINEARITY (%)

wfm ---> 5 STEP
PEAK-TO-PEAK = 1.4

105.0
104.5
104.0
103.5
103.0
102.5
102.0
101.5
101.0
100.5
100.0   100.0
99.5
99.0   99.1   99.1   99.8
98.5
98.0
97.9
97.5
97.0
96.5
96.0
95.5
95.0
      1ST   2ND   3RD   4TH   5TH
AVERAGE

FIGURE 32. LUMINANCE NON LINEARITY (PAL)

LINE FREQUENCY ERROR   0.00 (%)

     -0.4   -0.2   0.0   0.2   0.4
                         (%)

LINE FREQUENCY 15.625 (kHz)
FIELD FREQUENCY 50.00 (Hz)

AVERAGE OFF
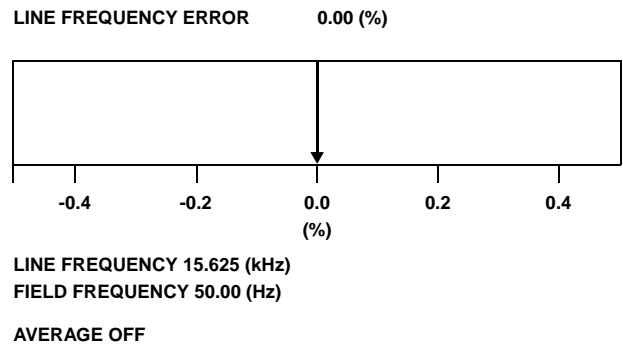
FIGURE 33. LINE FREQUENCY (PAL)

Typical Performance Curves (Continued)
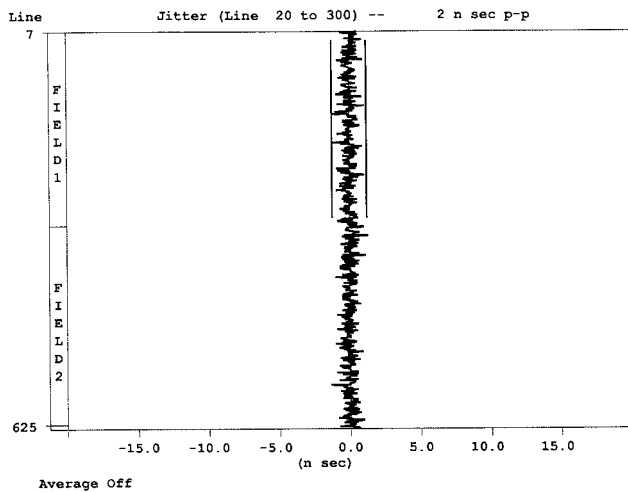
FIGURE 34. H SYNC JITTER IN A FRAME (PAL)
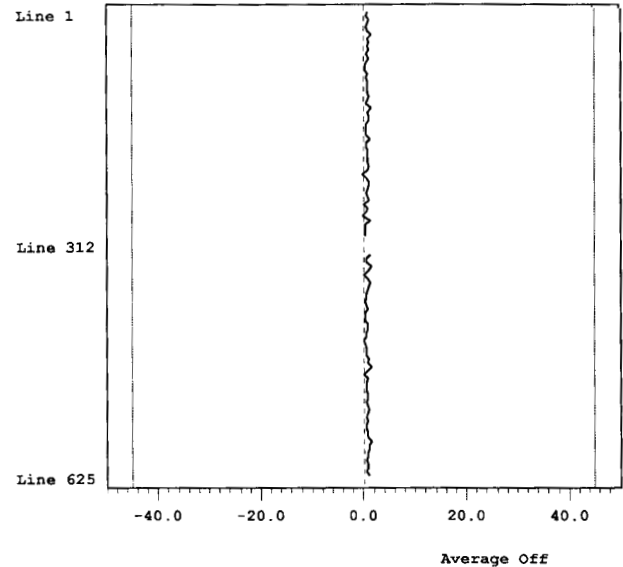
FIGURE 35. SCH PHASE MEASUREMENT (PAL)

Application Information

Vertical Blanking Information Encoding

VBI data such as teletext may be encoded on any line by driving the pixel inputs with appropriate data. For YCbCr input modes, Cb and Cr should equal 128 to disable the color information. For RGB input modes, R, G, and B should always have the same value to disable the color information.

Vertical blanking must be negated on the first scan line containing VBI information. If there are unused scan lines between the VBI data and active video, $\overline{BLANK}$ must remain on and the pixel inputs should be set to the black level.

Video Insertion Test Signalsy

Video test signals may be generated by driving the pixel inputs with appropriate data. Most of the video test signals require using YCbCr pixel data.

Vertical blanking must be negated on the first scan line containing video test signals. If there are unused scan lines between test signal data and active video, BLANK must remain off and the pixel inputs should be set to the black level.

PCB Considerations

A PCB board with a minimum of 4 layers is recommended, with layers 1 and 4 (top and bottom) for signals and layers 2 and 3 for power and ground. The PCB layout should implement the lowest possible noise on the power and ground planes by providing excellent decoupling. PCB trace lengths between groups of V_{AA} and GND pins should be as short as possible.

Component Placement

The optimum layout places the HMP8154/HMP8156A at the edge of the PCB and as close as possible to the video output connector. External components should be positioned as close as possible to the appropriate pin, ideally such that traces can be connected point to point. Chip capacitors are recommended where possible, with radial lead ceramic capacitors the second-best choice.

Traces containing digital signals should not be routed over, under, or adjacent to the analog output traces to minimize crosstalk. If this is not possible, coupling can be minimized by routing the digital signals at a 90 degree angle to the analog signals. The analog output traces should also not cross over or under the V_{CC} power plane to maximize high-frequency power supply rejection.

Power and Ground Planes

A common ground plane for all devices, including the HMP8154/HMP8156A, is recommended. However, placing the encoder on an electrically connected GND peninsula reduces noise levels. All GND pins on the HMP8154/HMP8156A must be connected to the ground plane. Typical power and ground planes are shown in Figure 36.

The small connection between the ground areas should be made wide enough so that most of the encoders digital inputs can be routed over or under it. It is especially important that the CLK and CLK2 signals cross through the connection.

The HMP8154/HMP8156A should have its own power plane that is isolated from the common power plane of the board, with a gap between the two power planes of at least 1/8 inch. All V_{AA} pins of the HMP8154/HMP8156A must be connected to this isolated power plane.

The HMP8154/HMP8156A power plane should be connected to the board's normal V_{CC} power plane at a single point though a low-resistance ferrite bead, such as a Ferroxcube 5659065-3B, Fair-Rite 2743001111, or TDK BF45-4001. The ferrite bead provides resistance to switching currents, improving the performance of HMP8154/HMP8156A. A single, large capacitor should also be used between the HMP8154/HMP8156A power plane and the ground plane to control low-frequency power supply ripple.
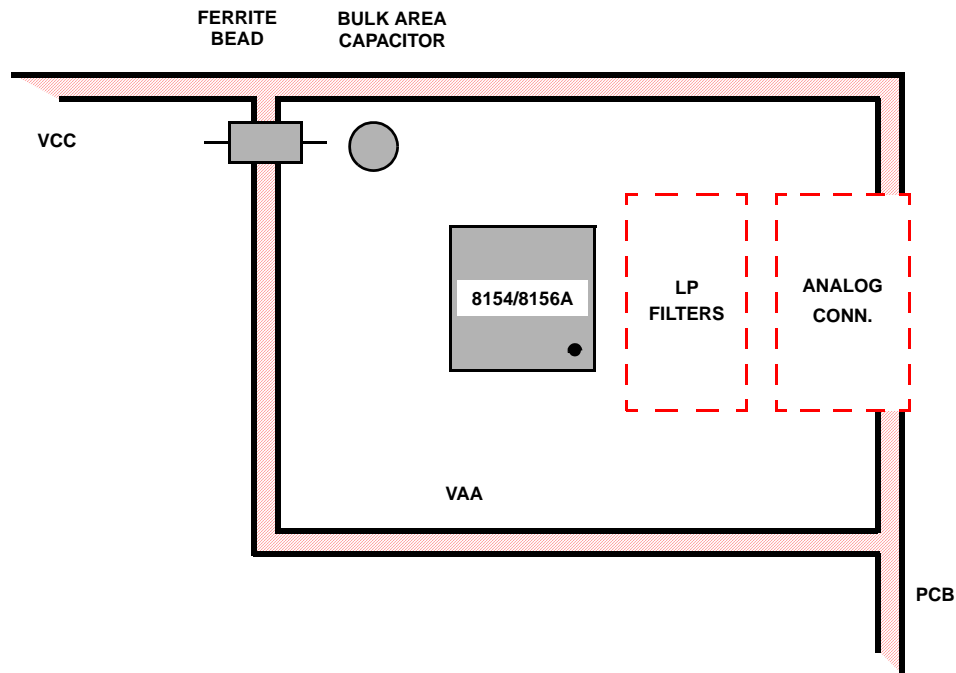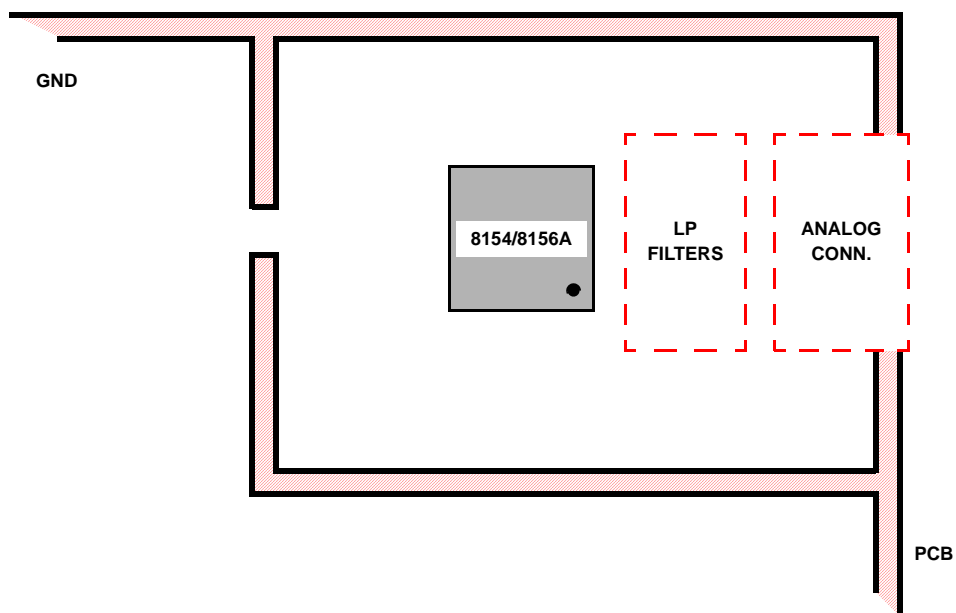
FIGURE 36A. V_{CC} AND V_{AA} PLANES

FIGURE 36B. COMMON GROUND PLANE

FIGURE 36. EXAMPLE POWER AND GROUND PLANES

For proper operation, power supply decoupling is required. It should be done using a 0.1μF ceramic capacitor in parallel with a 0.01μF chip capacitor for each group of V_{AA} pins to ground. These capacitors should be located as close to the V_{AA} and GND pins as possible, using short, wide traces.

If a separate linear regulator is used to provide power to the HMP8154/HMP8156A power plane, the power-up sequence should be designed to ensure latchup will not occur. A separate linear regulator is recommended if the power supply noise on

the V_{AA} pins exceeds 200mV. About 10% of the noise (that is less than 1MHz) on the V_{AA} pins will couple onto the analog outputs.

External Reference Voltage

If an external reference voltage is used, its circuitry should receive power from the same plane as the HMP8154/ HMP8156A. The external VREF must also be stable and well decoupled from the power plane. An example VREF circuit using a band gap reference diode is shown in Figure 37.
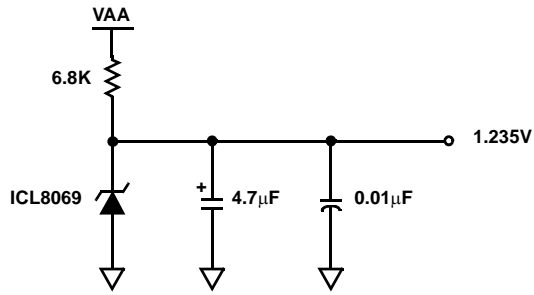
FIGURE 37. EXTERNAL REFERENCE VOLTAGE CIRCUIT

Analog Output Filters

The various video standards specify the frequency response of the video signal. The HMP8154/HMP8156A uses 2X oversampling DACs to simplify the reconstruction filter required. Example post filters are shown in Figure 38. The analog output filters should be as close as possible to the HMP8154/HMP8156A.
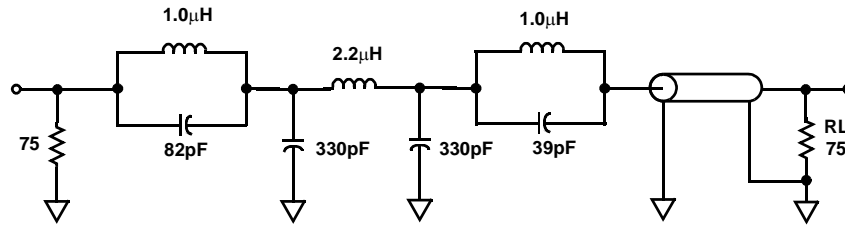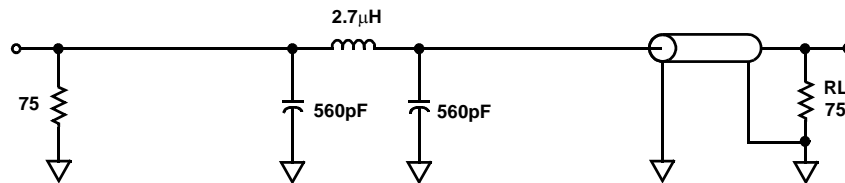

FIGURE 38A. HIGH QUALITY FILTER

FIGURE 38B. LOW COST FILTER

FIGURE 38. EXAMPLE POST-FILTER CIRCUITS

Evaluation Kits

The HMP8154EVAL1 is a small (index card size) printed circuit board containing the encoder, voltage references and bypassing, analog output filters, and input/output connectors. The board allows the encoder's operation and performance to be observed and measured.

The HMP8154EVAL1 board has a 50 pin, two row receptacle which allows connection into an existing system. The connector provides access to all of the encoder's digital inputs and outputs.

The HMP8156EVAL2 is the Intersil designed mother board for the HMP8154EVAL1. The mother board is a standard size PC add in card with an ISA bus interface and application software. The HMP8156EVAL2 kit is a complete system which allows demonstrating all of both encoders' operating modes. It has analog video inputs for composite,

S-video, and component RGB signals. The analog signals are converted/decoded to the digital domain and input to the encoder. The board also provides a 3 megabyte video RAM for image capture and display and a BT.656 connector and interface.

For simpler operation, the HMP8154EVAL1 may also be driven by external power supplies, a BT.656 signal generator, and a PC parallel port. The evaluation kit includes application software to program the part using its I2C bus connected to the printer port. The board includes the standard 25 pin BT.656 connector and interface.

Metric Plastic Quad Flatpack Packages (MQFP)
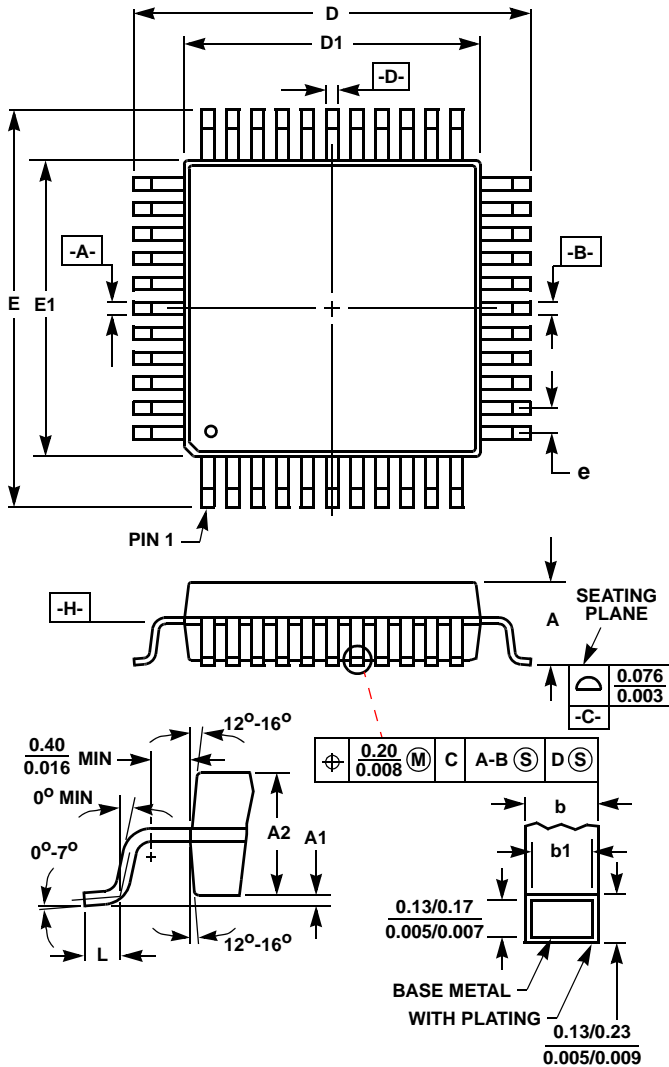
Q64.14x14 (JEDEC MS-022BE ISSUE B)
64 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.124	-	3.15	-
A1	0.004	0.010	0.10	0.25	-
A2	0.100	0.108	2.55	2.75	-
b	0.012	0.018	0.30	0.45	6
b1	0.012	0.016	0.30	0.40	-
D	0.672	0.682	17.08	17.32	3
D1	0.546	0.556	13.88	14.12	4, 5
E	0.673	0.681	17.10	17.30	3
E1	0.547	0.555	13.90	14.10	4, 5
L	0.029	0.040	0.73	1.03	-
N	64		64		7
e	0.032 BSC		0.80 BSC		-

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NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

2. All dimensions and tolerances per ANSI Y14.5M-1982.

3. Dimensions D and E to be determined at seating plane -C- .

4. Dimensions D1 and E1 to be determined at datum plane -H- .

5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.

6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.

7. "N" is the number of terminal positions.

For information regarding Intersil Corporation and its products, see www.intersil.com